INTERCONNECTS FOR POST-CMOS DEVICES: PHYSICAL LIMITS AND DEVICE AND CIRCUIT IMPLICATIONS

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Shaloo Rakheja

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INTERCONNECTS FOR POST-CMOS DEVICES: PHYSICAL LIMITS AND DEVICE AND CIRCUIT IMPLICATIONS

Approved by:

Professor Azad J. Naeemi, Advisor
School of Electrical and Computer Engineering
Georgia Institute of Technology

Professor Saibal Mukhopadhyay
School of Electrical and Computer Engineering
Georgia Institute of Technology

Professor James D. Meindl
School of Electrical and Computer Engineering
Georgia Institute of Technology

Professor Phillip N. First
School of Physics
Georgia Institute of Technology

Professor Jeffrey A. Davis
School of Electrical and Computer Engineering
Georgia Institute of Technology

Date Approved: December, 2012

For mom and dad

who taught me perseverance

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SUMMARY

The objective of this dissertation is to classify the opportunities, advantages, and limits of novel interconnects for post-CMOS logic that can augment or eventually replace the CMOS logic. Post-CMOS devices are envisaged on the idea of using state variables other than the electron charge to store and manipulate information. In the first component of the thesis, a comprehensive analysis of the performance and the energy dissipation of novel logic based on various state variables is conducted, and it is demonstrated that the interconnects will continue to be a major challenge even for post-CMOS logic.

The second component of the thesis is focused on the analysis of the interconnection aspects of spin-based logic. This research goal is accomplished through the development of physically-based models of spin-transport parameters for various metallic, semiconducting, and graphene nanoribbon interconnects by incorporating the impact of size effects for narrow cross-sectional dimensions of all-spin logic devices. Due to the generic nature of the models, they can be used in the analysis of spin-based devices to study their functionality and performance more accurately. The compact nature of the models allows them to be easily embedded into the developing CAD tools for spintronic logic. These models then provide the foundation for (i) analyzing the spin injection and transport efficiency in an all-spin logic circuit with various interconnect materials, and (ii) estimating the repeater-insertion requirements in all-spin logic, and (iii) estimating the maximum circuit size for all-spin logic. The research is crucial in pinpointing the implications of the physical limits of novel interconnects at the material, device, circuit, and architecture levels.

CHAPTER I

DIMENSIONAL SCALING

1.1 Introduction

The revolutionary growth of the silicon-based semiconductor industry has been supported by an increase in the binary information throughput resulting from the dimensional scaling of transistors on the microprocessor. Binary information throughput is a measure of the computation capability on the device level and is given as the number of transitions occurring per second per unit area in a microprocessor. However, dimensional scaling of devices is accompanied with an increase in the energy dissipation of the microprocessor. This increase in the energy dissipation of the microprocessor is expected to ultimately limit the extension of Moore's Law beyond the technology year 2024 [1]. Using materials other than silicon to implement field-effect transistors (FETs) will likely provide one-time performance gains, but these new FETs are expected to be limited by the same scaling laws that govern silicon FETs in complementary metal-oxide-semiconductor (CMOS) microprocessors [23]. Hence, alternative technologies, particularly those that use state variables other than the electronic charge, are highly desired. Some examples of novel state variables that are currently being investigated for post-CMOS devices include the electron spin, pseudospin in graphene, phonons, plasmons, magnetic-domain walls, and photons [68]. Novel devices must be able to communicate their new state variables in a fast and energy-efficient way at least at the local level of interconnections. Otherwise, the energy and circuit-area overhead needed for signal conversion would be prohibitive for the new technology. The search for promising novel state variables must, therefore, take communication into account. The aim of this research is to obtain comprehensive

physical models of the performance and the energy dissipation of novel interconnects for post-CMOS devices and to assess the implications of the physical limits of novel interconnects at the device, circuit, and architecture levels.

In this chapter, the primary background for this research project is presented. First, the impact of geometrical scaling of on-chip components (transistors and interconnects) on the performance and the energy dissipation of CMOS technology is reviewed. Second, an overview of the various novel state variables that are currently being explored by researchers is presented. Finally, the specific tasks undertaken in this research are described.

1.2 CMOS Technology

The semiconducting material silicon forms the heart of the current CMOS technology. Over the last four decades, the productivity of the silicon technology has increased by a factor of more than a billion [10]. This growth in the silicon technology was made possible by a steady reduction in the feature size, which helps to pack more functionality per cost in a microprocessor. Today, the silicon-based semiconductor industry is approximately a $270 billion market [10]. This exponential growth of the semiconductor industry was first pointed out by Dr. Gordon Moore. In 1965, Dr. Gordon Moore observed that the computing power of a microprocessor doubled every 18-24 months, and this observation later became known as Moore's Law [151]. In essence, Moore's Law is an economic law that serves to guide long-term planning and to set targets for research and development in the semiconductor industry. However, quantum-mechanical laws dictate that there are fundamental challenges associated with scaling on-chip components to below 10 nm [179]. Hence, a revolutionary innovation in semiconductor technology would be needed to sustain Moore's law for advanced technology nodes below 10 nm [1], [10].

In the next subsections, a review of the advantages and challenges of scaling

on-chip components in the CMOS technology is presented. The projections on the electrical parameters (resistance and capacitance) of devices and interconnects for future technology nodes have been taken from the International Technology Roadmap for Semiconductors (ITRS). The ITRS projections represent the consensus among semiconductor experts on the “best current estimate" of the research and development needs of the industry.

1.2.1 Geometrical scaling of CMOS transistors

The direct advantage of technology scaling is the improvement in the performance of transistors resulting from the increase in gate-control of the transistor channel. However, as transistor dimensions are scaled below 100 nm, many short-channel effects begin to diminish the improvement in the transistor speed. The dimensional scaling of transistors on a microprocessor is plagued with several challenges, such as the quantum mechanical tunneling through the gate oxide, the drain-induced-barrier lowering (DIBL), mobility degradation, and reliability problems [45]. However, for transistors, once these problems are overcome, their performance improves as a result of dimensional scaling. As seen from Figure 1, the intrinsic delay of the NFET is expected to be reduced from 0.8 ps to 0.17 ps as the technology scales from 45 nm in the year 2010 to 7.5 nm by the year 2024. The inset plot of Figure 1 shows the dynamic energy dissipation of switching an NFET versus the technology node. Since both the capacitance of the transistor and the supply voltage go down with technology scaling, the dynamic energy dissipation of the transistor decreases with technology scaling.

It is now well established that the fundamental limit of the energy dissipation of a single binary transition in a CMOS switch is $k_B T \ln 2$, where k_B is the Boltzmann constant, and T is the temperature of the system [143], [246], [32]. The minimum energy dissipation during binary switching in a CMOS transistor can be obtained by invoking the two-well model of the switch.

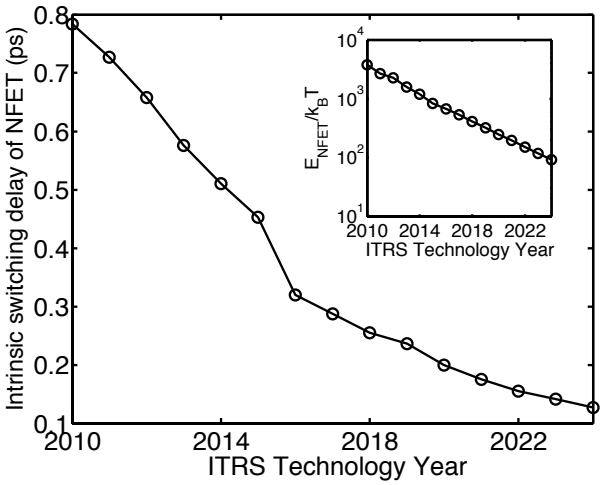

Figure 1: The intrinsic delay of NFET versus the ITRS technology year. The upper horizontal axis shows the minimum feature size (MFS) corresponding to the particular ITRS technology year. The inset plot shows the dynamic energy dissipation of NFET normalized to the thermal energy versus the ITRS technology year.

The CMOS switch shown in Figure 2 has two wells representing the source and the drain. The wells are separated by a potential barrier of height $V0$, which can be modulated by an external stimulus, such as the gate bias. The two stable states of the CMOS switch are labeled as *state 1* and *state 2* in the figure. Ideally, in the off-state of the switch, the potential barrier between the two states should be high enough to prevent spontaneous transition of the electron from one state to another, i.e., the two states must be distinguishable. Classically, the probability of spontaneous transitions over the barrier is given as

$$\Pi_{err} = exp\left(-\frac{V0}{k_BT}\right). \tag{1}$$

The distinguishability between the two states is lost when the probability of error, Π_{err}, exceeds 0.5. Using this condition, the minimum value of $V0$ between the two stable states must be equal to k_BTln2. Hence, any binary transition in the current charge-based CMOS transistor will have a minimum energy dissipation of k_BTln2.

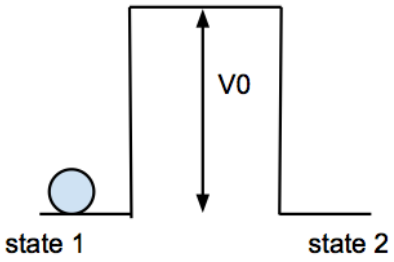

Figure 2: The two-well model used to describe a CMOS switch. The two stable states of the switch are labeled as *state 1* and *state 2*. The barrier height between the two stable states is denoted as V0.

1.2.2 Geometrical scaling of electrical interconnects

The dimensional scaling of on-chip interconnects degrades their performance and increases their energy dissipation relative to that of transistors. Interconnects also add noise and jitter to signals and are a major issue for gigascale integration. The interconnect delay problem can be explained effectively through two metrics: (i) signal-drive distance (SDD) and (ii) clock locality (CL). SDD is defined as the distance that a signal can travel through the interconnect in one-gate delay without using a buffer. CL is defined as the number of gate delays in one-clock cycle and dictates how far a signal can reach on the chip without the use of a synchronization register. Alternately, CL can also be expressed as the length of the interconnect that can be accessed in one-clock delay. The mathematical expressions of SDD and CL are given as

$$\mathrm{SDD} = -\frac{R_s}{r_w} + \sqrt{\left(\frac{R_s}{r_w}\right)^2 + \left(\frac{R_s}{r_w}\right)\left(\frac{C_s}{c_w}\right)}, \tag{2a}$$

$$\mathrm{CL} = -\frac{R_s c_w + r_w C_L}{r_w c_w} + \frac{\sqrt{(R_s c_w + r_w C_L)^2 - 1.5 r_w c_w \left(0.69\,(C_s + C_L)\,R_s - \frac{1}{f_{CLK}}\right)}}{0.69 r_w c_w}, \tag{2b}$$

where R_s and C_s are the source resistance and capacitance, respectively, r_w and c_w are the per-unit-length interconnect resistance and capacitance, respectively, C_L is

the load capacitance, and f_{CLK} is the clock frequency. Figure 3 shows the signal-drive distance versus the ITRS technology year for two values of the channel width-to-length ratio (W/L) of the CMOS driver: (i) W/L=1 and (ii) W/L=5. The signal-drive distance is less than two gate pitches at W/L=5, and it degrades continually as the technology scales from 45 nm to 7.5 nm. The inset plot of Figure 3 shows the clock locality in terms of the interconnect length accessed in one-clock delay versus the ITRS technology node. For W/L=5, the interconnect length accessed in one-clock delay drops from ≈ 300 gate pitches at 45 nm technology node to ≈ 150 gate pitches at 7.5 nm technology node. Because of the degradation in the performance of interconnects, both SDD and CL have degraded with technology scaling.

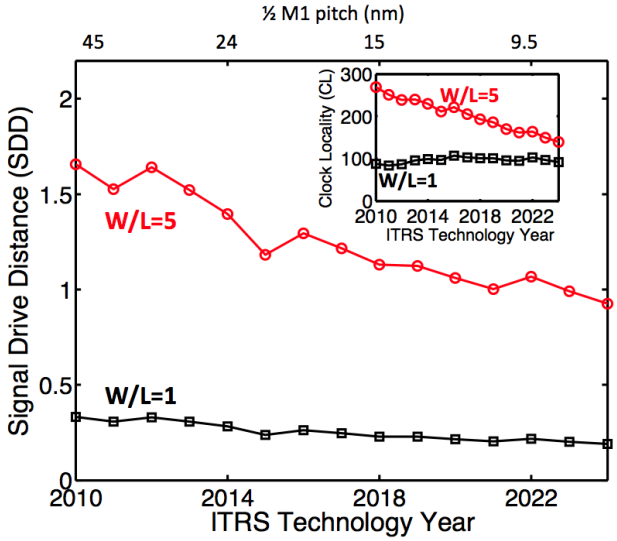

Figure 3: The signal-drive distance normalized to the gate pitch versus ITRS technology year for two inverter sizes: W/L=1 (minimum-sized inverter) and W/L=5 (5× the minimum-sized inverter). The inset plot shows clock locality normalized to the gate pitch versus ITRS technology year.

The energy dissipation in interconnects is associated with charging and discharging of the interconnect capacitance. Although the interconnect capacitance has reduced over the years, the energy dissipation of interconnects is still large compared to that of transistors. The length of the electrical interconnect whose energy dissipation is equal

to that of the CMOS transistor is plotted as a function of the ITRS technology year in Figure 4. This figure highlights the growing disparity in the energy dissipation of transistors and interconnects with technology scaling. It can be seen from this figure that interconnects as short as one gate pitch consume energy equal to that of minimum-sized transistors.

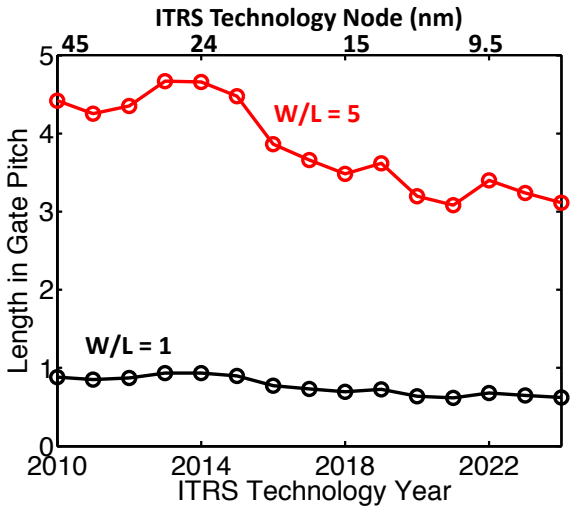

Figure 4: The length of the interconnect whose energy dissipation is equal to that of a CMOS inverter for two sizes of the inverter: (i)W/L=1 (minimum-sized inverter) and (ii)W/L=5 (5× the minimum-sized inverter).

To sustain Moore's Law beyond the 2024 technology node, less power-hungry computational systems are required. In particular, systems that use state variables other than electronic charge may introduce a paradigm shift and open up a new scaling path. The quest for a new switch in nanoelectronics must be partnered with an exploration of a suitable interconnect technology for the new logic. It is important to evaluate the interconnection aspects of the novel technology before making major investment into the research and development of the new technology.

1.3 Alternate State Variables

A state variable refers to the physical representation of information. In a charge-based CMOS technology, the state variable is the electronic charge; presence or absence of

charge is used to distinguish between the digital logic states of “1" and “0". Some examples of promising state variables for post-CMOS technology include

- spin orientation,
- pseudospin in graphene,
- magnetic-domain wall,
- spin waves,
- excitons,
- phonon, and
- plasmon.

1.3.1 Electron spin

Electron spin is a quantum mechanical property of the electron. Electron spin can align in one of the two quantization directions, which are conventionally known as spin-up and spin-down, permitting alternate representations of binary digits. Electronics using electron spin as the token of information is called spintronics. Recent interest in spintronics spurred from the discovery of the giant magnetoresistance (GMR) effect by Gruenberg and Fert in 1985 [66]. The discovery of the GMR effect led to renewed research efforts in tunnel magnetoresistance (TMR) [150], originally discovered at low temperatures in 1975 by M. Julliere [101]. The spin-valve effect forms the underlying principle of the GMR and the TMR effects. A spin valve is a magnetoelectronic device consisting of a non-magnetic layer sandwiched between two ferromagnetic layers as shown in Figure 5. The spin-valve device changes its resistance depending on the relative orientation of the two ferromagnetic layers [239]. In a spin valve, the magnetic orientation of the top ferromagnetic layer is pinned by the exchange coupling with an adjacent antiferromagnetic layer. The magnetic orientation of the free layer can be changed more easily upon application of a magnetic field. In a pseudo spin valve, the asymmetry between the pinned and the free layers

is generated by implementing the two magnetic layers with different materials so that the magnetization of the free layer switches more easily than that of the hard layer.

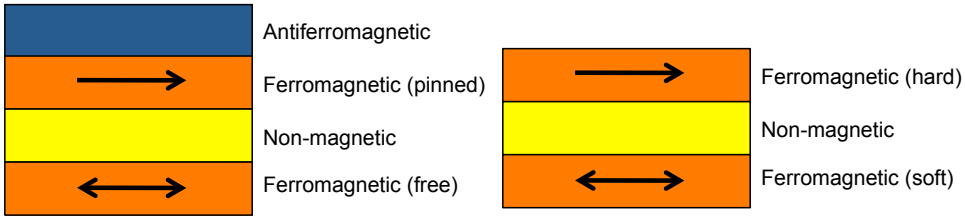

Figure 5: The figure on the left is a spin valve and the figure on the right depicts a pseudo spin valve.

The phenomena of spin valve has also been exploited to experimentally measure the spin-relaxation length in non-magnetic materials. Figure 6 shows an experiment set up to obtain spin-relaxation time in an aluminum channel. A four-terminal spin-valve geometry with cobalt electrodes is used in the experiment to measure the non-local spin-valve signal at the electrode labeled Co2 in the figure. The absolute value of the non-local spin-valve signal at Co2 contains information about the polarization of the spin signal and the spin-relaxation length in the aluminum channel. Both GMR and TMR effects have also been used as the underlying mechanism in implementing magnetic random-access memories (MRAMs) [90]. Another spin-based phenomena, the spin-torque effect, has been used to implement spin-transfer-torque (STT) memories [85]. Spin torque refers to the phenomena in which a spin-polarized current deposits its spin angular momentum as it passes through a small magnetic conductor [215]. As a result, the magnetization of the magnetic conductor will undergo precession or may even switch its direction (see Figure 7). Recently, there have been promising proposals that use the spin-torque effect when implementing all-spin logic (ASL) [14]. In an all-spin logic, a non-local spin-valve geometry is used with nanomagnets serving as the injecting and detecting electrodes. A review of the potential applications of spintronics for future logic and universal memory is provided in [61] and [253].

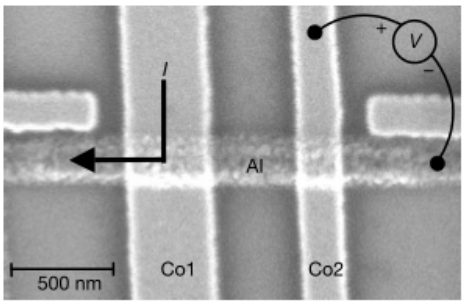

Figure 6: Geometry of the spin valve by Jedema et al [93]. The channel is implemented with aluminum, while cobalt serves as both the injector and the detector. The voltage is measured between the electrode Co2 and the right side of the aluminum strip.

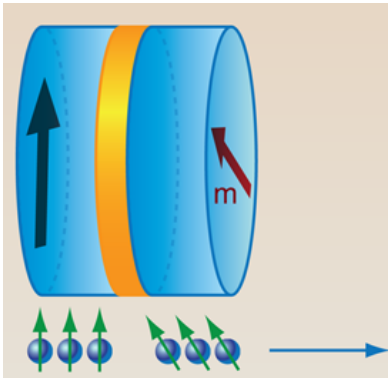

Figure 7: A nanopillar structure in which the right layer, which is the free layer, may be switched by the spin torque of the spin-polarized current entering it. The polarization of the current also rotates as a result of the spin-torque effect [214].

1.3.2 Pseudospin in graphene

Graphene is a two-dimensional semiconductor with a zero energy gap and a linear energy-dispersion relation near the Dirac point (see Figure 8). The honeycomb lattice of graphene is composed of two sublattices. To describe the low-energy quasi-particles in graphene, the Dirac-like Hamiltonian is used [71]. The Hamiltonian for graphene is given as

$$\hat{H} = \hbar v_f \begin{pmatrix} 0 & k_x - ik_y \\ k_x + ik_y & 0 \end{pmatrix} = \hbar v_f \vec{\sigma}.\vec{k}, \tag{3}$$

where $\hbar$ is the reduced Planck's constant, v_f is the momentum-independent Fermi velocity, $\vec{\sigma}$ is the 2D Pauli matrix, and $\vec{k}$ is the particle momentum. Near zero energy, the electronic states are composed of states belonging to the two sublattices as illustrated in Figure 8. An index is needed to distinguish the contribution of the two sublattices to the overall wavefunction. This index is called the pseudospin. In Eq. (3), $\vec{\sigma}$ denotes the pseudospin in graphene. The phase shifts between the wavefunctions of electrons residing in the two sublattice sites provide a spin-like opportunity in graphene and may be used as a new token of information [98]. Pseudospintronics in graphene is a promising new field that provides pseudospin version of giant magnetoresistance and spin-torque effect. Recently, S. Jose [98] proposed a pseudospin valve in bilayer graphene (BLG) in which the polarity of a control voltage is used to switch the direction of pseudospin. This opens up future possibilities of exploiting the pseudospin degree of freedom in graphene to build a new digital switch.

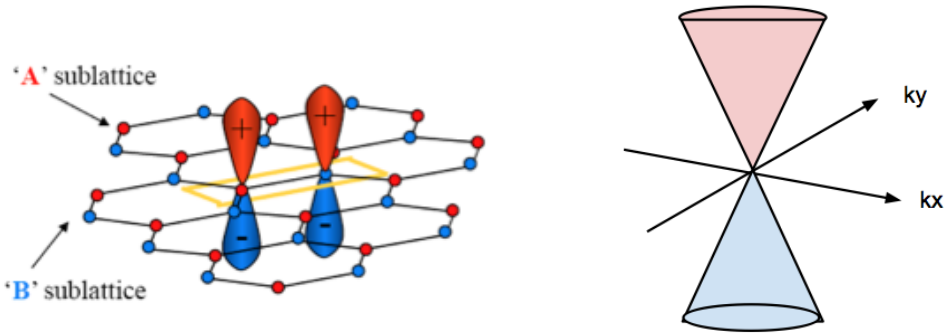

Figure 8: The figure on the left shows the two sublattices in graphene. The figure on the right shows the energy-dispersion relation of 2D graphene.

1.3.3 Magnetic-domain wall

A magnetic-domain wall is a mobile interface between regions of opposite magnetic orientations [231]. A domain wall may be induced by an external magnetic field or by a spin-polarized current utilizing the concept of spin-transfer torque [245], [18]. Magnetic material Permalloy (NiFe) is an excellent candidate to implement domain-wall

interconnects. Experiments in domain-wall motion have been conducted in systems with either an in-plane or a perpendicular magnetization. In 2005, it was shown by D.A. Allwood that domain walls may be used to represent digital logic in a spintronic system [2]. For instance, in the case of nanowires, their high shape anisotropy ensures that the magnetization aligns along their long axis. Logic “1" may be defined as the magnetization pointing in the direction of the propagating domain wall and logic “0" as the magnetization opposing the propagation of the domain wall.

1.3.4 Spin waves

A spin wave is a collective oscillation of electron spins in an ordered spin lattice around the direction of magnetization [108]. In spin waves, information is encoded into the phase or the amplitude of the spin wave. The underlying idea of the spin wave is to establish communication between inductively-coupled devices using a magnetic flux rather than a current flow through wires. Ferromagnetic interconnects such as NiFe or CoFe can be used as conduits of spin waves [106].

1.3.5 Exciton

An exciton is a quantum-coupled electron-hole pair in the periodic structure of the crystal. There are typically two kinds of excitons: direct and indirect. In the case of direct excitons, both the electron and the hole are located at the same physical location in the crystal; thus, the wavefunctions of the electrons and the holes overlap, which makes it easier for the electron and the hole to recombine quickly. As such, direct excitons are quite short-lived at room temperature. Indirect excitons can be created by the application of an external electric field that serves to separate the electron and the hole in the crystal. Therefore, the lifetime of the indirect excitons is more than that of the direct excitons. The spin degree of freedom of excitons or their presence and absence may be used as the token of information [50], [211].

1.3.6 Phonon

Heat carriers or phonons in a crystal may also be used to carry information in a system. A thermal diode that allows heat flow preferentially in one direction was first proposed in 2004 by Li et al [124]. A theoretical proposal of thermal rectification in nanotubes was put forth by Chang et al [34] followed with a proposal on thermal rectification in asymmetric graphene nanoribbons by Hu et al [86]. To use phonons as information carriers in logic, nonlinear lattices that have a temperature-dependent power spectra are required [121]. Negative temperature-differential resistance, which is a necessary principle for thermal transistor, was simulated in a one-dimensional Frenkel-Kontorova lattice by Wang and Baowen [131].

1.3.7 Plasmon

Surface plasmons were widely recognized in the field of surface science following the pioneering work of Ritchie in the 1960's [185]. Surface plasmons are light waves that propagate along the surface of a conductor that is usually a metal. A plasmon can be viewed as a coupled electron and light oscillation, also known as Òlangmuir wavesÓ. Surface plasmon waves are polarized in the transverse-magnetic direction [133]. Silver is the material of choice for a plasmonic conductor since it offers the lowest ohmic loss over a wide frequency spectrum [13]. The most attractive feature of plasmons over conventional dielectric devices is their ability to confine light to below the diffraction limit and realize high field intensities in relatively small volumes. This could help to miniaturize photonic circuits that have typically been much larger than their electronic counterparts. Plasmonic waveguides can also be used to propagate light and serve as the interconnect for plasmonic circuits. However, plasmonic switches are needed to implement a plasmon-based computation system; otherwise, the overhead associated with signal conversion (energy and circuit-area overhead) will be prohibitive for the plasmonic technology.

1.4 Thesis overview

Any information-processing system is built with a certain set of inputs and outputs; switches to store and manipulate information and interconnections to communicate information. The quintessential job of interconnects is to transmit information between different physical locations on the chip. Any novel technology that aims to augment or to eventually replace the CMOS technology must be complemented with a suitable interconnect technology to help communicate information on the chip. While most of the research in alternate state variables is focused on the device aspects, little research has been conducted in the interconnection aspects of various novel technologies. Realizing that communication of information is at the heart of any information-processing system, following interconnect-oriented tasks are undertaken in this research:

1. developing physical models of the performance of various novel interconnects
2. developing physical models of the energy dissipation of various novel interconnects
3. developing models of transport parameters in various spin-interconnect materials: copper, aluminum, graphene, silicon, gallium arsenide
4. developing models of spin-relaxation length as a function of interconnect dimensions
5. spin injection and transport efficiency in all-spin logic
6. circuit-level and system-level analyses of spin logic: energy-delay tradeoff and quantifying repeater-insertion requirements

A brief description of the various tasks is given below.

Tasks I and II: In Chapter II, models of the performance and the energy dissipation of novel interconnects as a function of interconnect length for various new digital logic systems are developed. The delay and the energy dissipation of novel interconnects are compared against those of their CMOS counterparts at the 2024 technology node (corresponding to a minimum feature size of 7.5 nm).

Task III: Amongst the various new state variables, electron spin is the most studied with proven advantages in terms of robustness, non-volatility, and energy dissipation [9]. Interconnects for propagating spin-based information via spin currents are analyzed in Chapter III. Various interconnect options are considered: metallic conductors (copper and aluminum), two-dimensional graphene, and doped semiconductors (silicon and gallium arsenide). The transport parameters that affect the performance and the energy dissipation of spin interconnects are modeled as a function of interconnect dimensions in the presence of size effects.

Task IV: Unlike charge current, spin current is not a conserved quantity. The spin current continually degrades as it flows within the interconnect because of spontaneous spin-flipping processes. The degradation in spin current is captured through the spin-relaxation length, which is a function of temperature, size effects, and doping concentration (for semiconducting spin interconnects). In Chapter IV, physical models of spin relaxation in various spin-interconnect materials are developed as a function of interconnect dimensions, temperature, doping type and doping concentration.

Task V: An important figure of merit for all-spin logic circuits is the spin injection and transport efficiency (SITE) that specifies the amount of spin-polarized current available at the receiver for signal detection. In the ideal case, the SITE of the all-spin logic circuit should be equal to the conductivity polarization of the injection ferromagnet according to the spin-diffusion formalism. However, the injection of spins from the ferromagnet into the interconnect is not ideal and introduces losses in the spin signal. In addition, random spin-flipping processes occurring in the interconnect tend to destroy the spin information before it reaches the receiver nanomagnet, especially if the interconnect length is longer than the spin-relaxation length in the interconnect. Hence, the transport of the spin signal introduces additional losses in the spin signal; the transport loss strongly increases with an increase in the interconnect length. The SITE of the all-spin logic circuit captures the effects of both injection and transport

losses in the spin signal. In Chapter V, the SITE of the all-spin logic is determined for various interconnect materials. The impact of nanomagnet polarization, interconnect length, and the dimensional scaling on the SITE is examined.

Task VI: Circuit-level analysis of a spin-torque circuit with nanomagnet injector and detector is provided in Chapter VI. Spin repeaters must be inserted along the interconnect to boost the spin signal. An optimal repeater-insertion frequency is determined for the all-spin logic circuit that minimizes the delay of the circuit. Using the optimal repeater-insertion frequency, the input electrical current in the all-spin logic circuit is optimized to provide the lowest energy dissipation. Both the performance and the energy dissipation of the all-spin logic circuit and the CMOS circuit are compared at the 2024 ITRS technology node. Energy-delay tradeoff of spin circuits is compared with that of CMOS circuits at the 2024 technology node. It is established that both the delay and the energy dissipation of interconnects in both electrical and spin domain are highly dependent on the interconnect length. Any logic circuit has interconnects with drastically different lengths, where wire-length distribution is a function of the circuit architecture and circuit complexity. The stochastic wire-length distribution models are based on Rent's rule that relates the number of input/output pins to the number of gates in a hypothetical logic block [144]. The stochastic wire-length distribution models are rigorously obtained for a square array of homogenous logic gates in [43], [44]. These wire-length distribution models determine the wire-length frequency and "a priori estimation of the wiring requirements for future GSI chips." In Chapter VI, using stochastic wire-length distribution models, the dependence of the average performance and the energy dissipation on the number of gates in the random logic are obtained for all-spin logic with various interconnect materials. An upper bound on the circuit size for all-spin logic is determined when it is assumed that only a certain fraction of the total number of gates in the logic are dedicated as repeaters. The impact of circuit complexity, captured through Rent's exponent, on

the maximum circuit size of all-spin logic with graphene nanoribbon interconnects is studied. Further, the impact of dimensional scaling and the spin-relaxation length on the maximum circuit size is also analyzed.

The compact physics-based models for the performance and energy dissipation of novel interconnects developed in this research project will serve to guide future research in emerging spintronic circuits by examining the implications of the physical limits of interconnects at the device, circuit, and architecture levels for novel logic.

CHAPTER II

PHYSICAL MODELS OF PERFORMANCE AND ENERGY DISSIPATION OF NOVEL INTERCONNECTS

Followed by several decades of exponential scaling, CMOS transistors are expected to approach their scaling limit around the technology year 2024 [1]. Power dissipation is considered as the main limit, and the energy dissipation in CMOS transistors is projected to approach the $k_B T$ limit that is dictated by thermal noise [33]. Here, k_B is the Boltzmann's constant, and T is the temperature in Kelvin. All field-effect switches are expected to eventually face the same power-dissipation limit imposed by thermal noise [102]. To overcome this power barrier in CMOS switches, state variables other than electronic charge are being explored to invent new devices that can augment or even replace the conventional CMOS nanoelectronics. Some examples of novel state variables are electron spin, presence or absence of electron-hole pairs called excitons, and pseudospin in graphene [68]. It has been demonstrated that the novel state variable must be used as both the input and the output of the new switches. Otherwise, if the state variable is used solely to control the current flow, the same thermal noise limitation will be applicable to the new devices [9]. Therefore, interconnects for new devices must provide a medium to communicate information encoded in the new state variable at least locally. Otherwise, the energy and circuit-area overheads needed for signal conversion will be prohibitive for the new technology.

Virtually all of the current research on post-CMOS logic is focused on switches, and little research has been conducted on the interconnect aspect of the new logic. In CMOS circuits, more than half of the capacitance on a chip is associated with wires because of which more than 50% of the dynamic power dissipation on a chip is due to

interconnects [135]. Furthermore, continued scaling of on-chip wire cross sections has caused interconnects to become the dominant component in the critical-path delay of circuits [154]. The fact that interconnects are the major limits for power efficiency and performance of Si CMOS chips underscores that interconnects cannot be treated as an afterthought in the search for new information-processing elements. Hence, a systematic understanding of the interconnect limits and opportunities offered by new state variables and their circuit and system impacts are critically needed.

This chapter is divided into four sections. In Section I, the performance and the energy dissipation of CMOS interconnects at the 2024 ITRS technology year is discussed. In Section II, various transport mechanisms for post-CMOS devices are detailed, and their performance and energy-per-bit models are developed as a function of interconnect length. A comparative analysis of CMOS and novel interconnects is also provided in this section. In Section III, the concept of "area scaling" for novel interconnects is introduced, and area-scaling factors required of various novel interconnects to match in performance with CMOS interconnects are quantified. Also, system-level communication metrics such as signal-drive distance, clock locality, square-bandwidth per unit area are quantified for novel interconnects and compared against those of their CMOS counterparts.

2.1 The CMOS Interconnect

The quintessential purpose of an interconnect is to communicate information between different physical locations on the chip with minimum latency [144]. Physically, electrical interconnects are patterned metal layers atop a dielectric or within a dielectric. In current CMOS technology, interconnects are implemented in copper with an intra/inter-layer dielectric. The dielectric is typically an oxide with low effective dielectric constant ($\kappa_{\mathsf{eff}} \leq 3$.) The use of copper interconnects in microprocessors was

introduced at the 220 nm technology node. The damascene process to pattern copper interconnects has played a pivotal role in the success of the copper-interconnect technology [3], [4]. Copper damascene process is essentially a four-step process, that begins with patterning the dielectric using photomasks and lithography techniques. The second step consists of the deposition of a barrier layer such as Ta or TiN over the patterned dielectric in order to prevent the metal and dielectric interaction. This is especially important because diffusion of copper into the dielectric creates a deep impurity level that degrades the device performance. The third step consists in filling the pattern with metal using electrochemical deposition. As the last step, chemical mechanical polishing is done to remove excess copper to planarize the metal surface. The process steps in a typical Cu damascene process are illustrated in Figure 9. The drive towards lowering the effective dielectric constant to minimize the wire capacitance has significant difficulties associated with manufacturing, cost, and reliability. A hybrid of porous low-κ dielectrics with air gap technology may be incorporated in the future process flow in order to sustain the drive towards lower dielectric constant [1].

The effective resistivity of Cu/low-κ interconnects in the presence of line-edge roughness and scatterings (grain-boundary and sidewall) is given as [129]

$$\rho_{eff} = \frac{\rho_0}{\sqrt{1-(u/W)^2}} \left(GB_{scat} + 0.45(1-p)\frac{\lambda}{W}\left(W/T + \left(1-(u/W)^2\right)\right)\right), \qquad (4)$$

where ρ_0 is the bulk conductor resistivity, u is the line-edge roughness, λ is the bulk mean free path (MFP) of the electrons in the interconnect material, W is the interconnect width, T is the thickness of the interconnect, p is the sidewall-specularity parameter, and GB_{scat} defines the impact of grain-boundary scattering on the effective resistivity. GB_{scat} is given as

$$GB_{scat} = \frac{1}{3}\left[\frac{1}{3} - \frac{\alpha}{2} + \alpha^2 - \alpha^3 \ln\left(1+\frac{1}{\alpha}\right)\right]^{-1}, \qquad (5a)$$

$$\alpha = \frac{\lambda}{d}\frac{R}{1-R}, \qquad (5b)$$

where d is the average separation of the grain boundaries, and R is the fraction of electrons scattered by the potential barrier at the grain boundary. The separation between the grain boundaries, d, is assumed to be equal to the interconnect width. Figure 10 shows the effective resistivity of Cu normalized to its bulk resistivity as a function of the line-width of the metal for different values of side wall specularity, grain boundary reflectivity, and line edge roughness. This figure shows that the cumulative impact of size effects is to increase the effective resistivity of the interconnect, thereby deteriorating its performance.

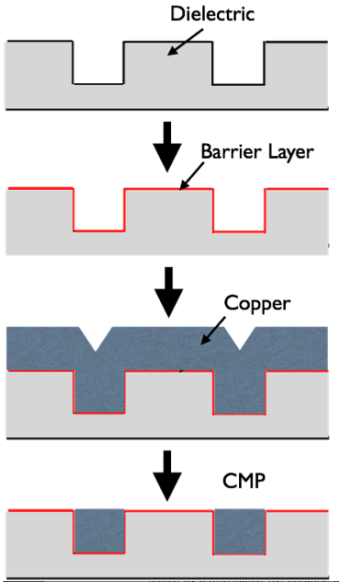

Figure 9: Cu damascene process.

Consider the CMOS system depicted in Figure 11. The interconnect can be represented by a distributed RC network, and the delay of this system is given as [11]

$$t_{CMOS} = 0.69R_s\left(C_s + C_L\right) + 0.69\left(R_s c_w + r_w C_L\right)L + 0.38 r_w c_w L^2. \tag{6}$$

The symbols used in Eq. (6) and their meanings are given in Table 1.

Figure 12 shows the delay associated with different terms in Eq. (6) for an interconnect driven by a driver with 5× the strength of a minimum-sized driver (also termed "5×" driver) at the 2024 technology node.

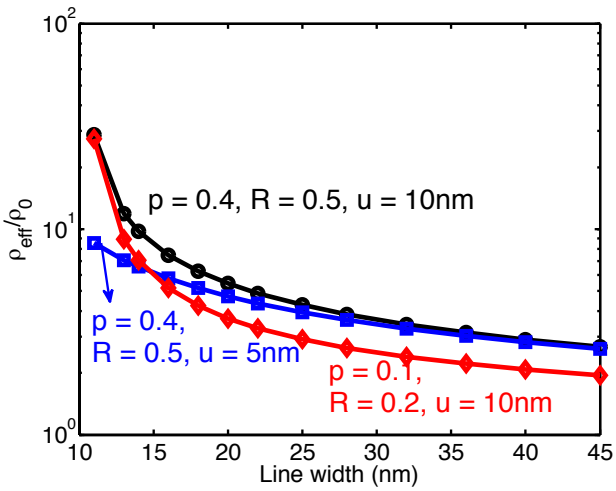

Figure 10: Resistivity of Cu line normalized to the bulk resistivity of Cu versus linewidth.

Table 1: Values of the resistance and the capacitance of devices and interconnects to evaluate the delay of the CMOS circuit at the 2024 technology node [1].

Symbol	Meaning	Value
W	Width taken equal to 1/2 metal-1 (M1) pitch	7.5nm
V_{DD}	Supply voltage	0.6V
I_{DSAT}	Saturation current of min.-sized NFET	$2170\mu A/\mu m$
R_s	On-resistance of min.-sized inverter = $V_{DD}/(I_{DSAT} \times W)$	$37k\Omega$
C_s	Parasitic capacitance of minimum-sized inverter	6.3aF
C_L	Load capacitance of minimum-sized inverter	6.3aF
c_w	Per-unit-length capacitance of local-level M1	1.2pF/cm
AR	Aspect-ratio = height/width	2.1
H	Height of the interconnect	15nm
r_w	Per-unit-length resistance of local-level M1	$2.72 \times 10^7 \Omega/cm$

For simulations, the reflectivity, R, is taken to be 0.5; the specularity, p, is assumed to be 0.5; the line-edge roughness, u, is taken to be 40% of the interconnect width. With these parameters, the effective resistivity of Cu is $2.39\times10^{-5}\Omega.m$, which is more than 10× higher than the value of its bulk resistivity. The delay-versus-interconnect-length landscape in Figure 12 has been partitioned into four distinct regions. Region I in Figure 12 is labelled as the sub-linear region. In this region, the impact of the term $R_s\,(C_s + C_L)$ is comparable to the impact of the term $R_s c_w L$. Region I covers only very short interconnects up to a length of six gate pitches. In Region II, the

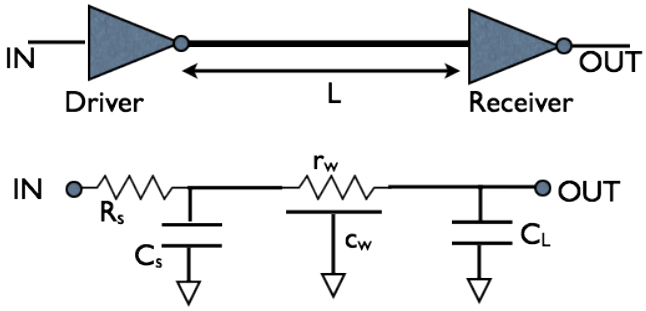

Figure 11: The schematic of the CMOS system with a CMOS driver, an interconnect, and a CMOS load (top). The equivalent circuit representation of the CMOS system (bottom).

overall delay follows very closely the term $R_s c_w L$, and the effect of other terms on the total delay can be ignored. This region is labelled as the linear region, and it spans interconnects of length six gate pitches to 30 gate pitches. For interconnects longer than 30 gate pitches, the effect of the term $r_w c_w L^2$ on the overall delay becomes non-negligible in comparison to the term $R_s c_w L$. The region spanning interconnects of length 30 to 200 gate pitches is labelled as the super-linear region. In Region IV, the total delay is dominated by the term $r_w c_w L^2$, and this region is labelled as the quadratic region. The boundaries between the different regions in the delay-versus-interconnect-length landscape depend both on the strength of the CMOS driver driving the interconnect and the technology parameters. The focus of this research is on short, local interconnects; therefore, only interconnects up to 100 gate pitches will be considered in the following analyses.

The energy dissipation of the CMOS system shown in Figure 11 is given as the amount of energy needed by the supply voltage, V_{DD}, to charge the capacitance at the output node of the driver. The output capacitance at the driver is the sum of its parasitic capacitance, the interconnect capacitance, and the load capacitance. The

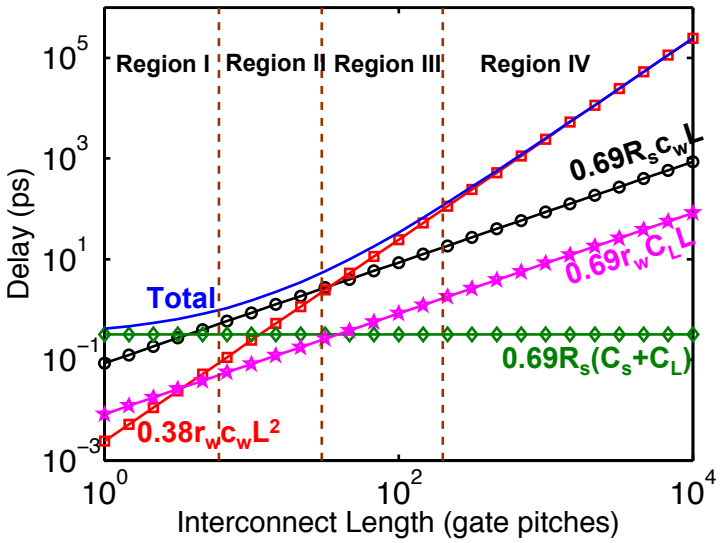

Figure 12: Delay associated with the different components in the CMOS system (see Eq. (6)) for a CMOS interconnect driven by a 5× driver at the 2024 technology node (F=7.5nm).

net energy dissipation of the CMOS system is given as

$$E_{CMOS} = \frac{1}{2}\left(C_s + c_w L + C_L\right) V_{DD}^2. \tag{7}$$

The symbols in Eq. (7) have the same meaning and the values as given in Table 1. Figure 13 shows the energy dissipation associated with different terms in Eq. (7) for an interconnect driven by a 5× driver at the 2024 ITRS technology year. It can be seen from Figure 13 that the energy consumed in charging/discharging the interconnect capacitance exceeds the energy consumed in charging/discharging the source parasitic and load capacitances for interconnects as short as four gate pitches. Thus, for interconnects longer than four gate pitches, the net energy dissipation being governed by the interconnect energy dissipation, becomes linearly dependent on the interconnect length.

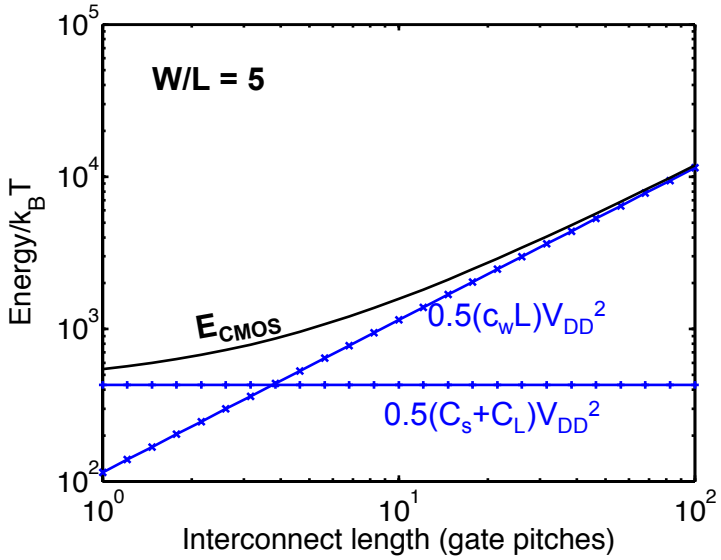

Figure 13: Energy dissipation versus interconnect length for the CMOS system with a 5× driver.

2.2 Novel Interconnects

Currently there are many state variables for post-CMOS logic that are being explored as alternatives to the electronic charge. As the first step towards modeling the physical limits of novel interconnects, a mapping between the state variable and its corresponding physical transport mode that can communicate information encoded in the particular state variable is established. This map is shown in Table 2. This map provides a generic platform to compare the interconnection aspects of various alternate state variables simultaneously and benchmark them against their conventional CMOS counterparts.

Communication between devices on the chip can be established by physically transporting the information token or by wave propagation between devices. Thus, transport modes can be broadly categorized into particle-based and wave-based communication. Particle-based communication mechanisms include diffusion, drift, and ballistic transport. Information can also be communicated via plasmonic waves, spin waves, and electromagnetic waves.

Table 2: A map of the physical transport mechanism and the corresponding state variable for which the transport mechanism can potentially be used to establish communication between the on-chip driver and the receiver.

Transport Mode	**Information Token/State Variable**
Diffusion	Spin, Pseudo-spin, Temperature (Phonons), Direct-excitons, Indirect-excitons
Drift	Indirect-excitons, Spin, Pseudo-spin
Ballistic	Spin, Pseudo-spin, Temperature (Phonons)
Spin Waves	Spin
Electromagnetic Waves	Photons, Plasmons

2.2.1 Particle-based interconnects

In this section, compact physical models of performance and energy-per-bit of particle-based interconnects as a function of their length are obtained. The particle-based interconnects include diffusion, drift, and ballistic interconnects.

2.2.1.1 Diffusion interconnects

Diffusion is a “kinetic" process in which particles (called “carriers" hereafter) move from a region of high concentration to a region of low concentration. The process of diffusion is governed only by the concentration gradient in the region and does not require any external forces to act upon the carriers. Hence, diffusion may be used for a variety of state variables including those that do not have a net charge associated with them, and, therefore, cannot be manipulated with an external electric field. As shown in Table 2, diffusion can be used for communicating information encoded in electron spin, pseudospin in graphene, both direct and indirect excitons, and phonons. In this thesis, we present the models of delay and energy dissipation for diffusion interconnects in spin-based and phonon-based computation systems. The models are

generic and can very easily be applied to other state variables that use diffusion as the transport mode for information communication.

Spin-based diffusion interconnects: In the case of spin, if the driver injects electrons with a certain spin polarization and removes the same number of electrons with opposite spin polarization, a concentration gradient will be set up in the interconnect without any charge accumulation. This will drive the diffusion of spins in the interconnect. A non-local spin-torque (NLST) device is used as the prototype of a switching element in the spin domain. The NLST device is shown in Figure 14. The transmitter in the NLST consists of nanomagnetic electrodes labeled as C1T and C2T and the non-magnetic interconnect of length L_1 sandwiched between C1T and C2T. The interconnect may be implemented with conventional metals like copper or aluminum, or a carbon-based material such as graphene nanoribbon, or even doped semiconductors like silicon (Si) and gallium arsenide (GaAs). An electrical current, I_{elec}, is used to pump spin-polarized electrons underneath FM-1 into the interconnect through a high-resistance barrier. The barrier is usually implemented with Al_2O_3 or MgO. A pure spin-diffusion current flows through the interconnect. The receiver nanomagnet is labelled as FM-3, and it forms an ohmic contact with the interconnect without any high-resistance barrier. This reduces the back-injection of carriers from the receiver into the interconnect. Upon reaching the receiver, the spin current may flip the magnetization of the receiver nanomagnet via the spin-torque effect.

The one-dimensional partial differential equation governing the transport of spins through the interconnect is given as

$$\frac{\partial s}{\partial t} = D\frac{\partial s}{\partial x^2} - \frac{s}{\tau_s}, \tag{8}$$

where s is the concentration of electron spins in $1/cm$, D is the diffusion coefficient of electron spins in the interconnect in cm^2/s, and τ_s is the spin-relaxation time in

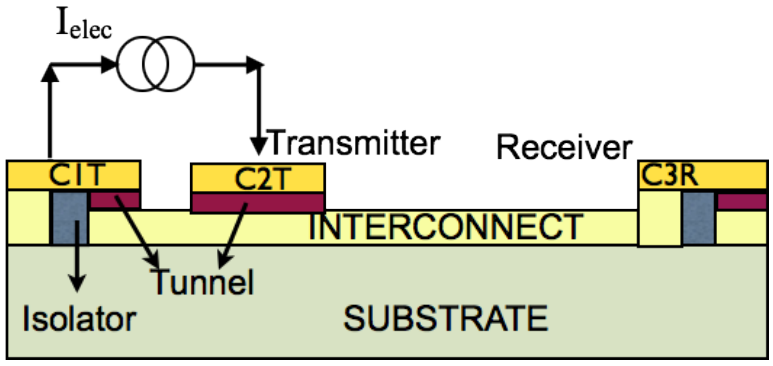

Figure 14: A non-local spin torque device. Spin diffusion current flows through the interconnect to establish communication between the transmitter and the receiver.

s. To obtain an upper bound on the speed of spin-diffusion interconnects, it is initially assumed that the spin relaxation in the interconnect is negligible in the time it takes for the carriers to diffuse from the transmitter to the receiver. Mathematically, $L^2/D << \tau_s$. This assumption is later relaxed in Chapter VI. The boundary conditions to obtain the solution of Eq. (8) are

$$s(x, t = 0) = 0, \tag{9a}$$

$$-D\frac{\partial s}{\partial x} = \eta I_{elec}, \tag{9b}$$

$$s(x = L, t) = 0. \tag{9c}$$

In Eq. (9b), η denotes the efficiency of spin injection. The efficiency of spin injection gives the amount of spin current injected at the beginning of the interconnect flowing towards the receiver for a given input electrical current. The spin-injection efficiency is a function of the circuit parameters such as the nanomagnet and interconnect resistance. Mathematical models of the spin-injection efficiency as a function of circuit parameters (circuit dimensions and size effects) are developed in Chapter V. At this time, the time-dependent solution of Eq. (8) is plotted in Figure 15 assuming $\eta = 1$.

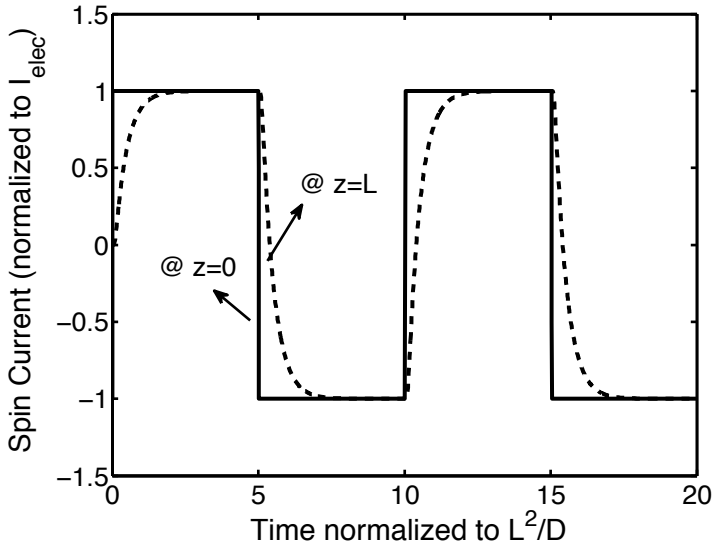

Figure 15: Time evolution of the spin-diffusion current at the receiver (dashed). Spin current at the beginning of the interconnect is assumed to have an infinitesimally small rise time (solid).

The time taken for the spin current in the interconnect to reach its steady state is given as

$$t_{DIFF,spin} = \frac{L^2}{2D}. \tag{10}$$

The values of electron diffusion coefficient in various non-magnetic materials are collected from experiments and tabulated in Table 3. The diffusion coefficient of electrons depends on (i) interconnect dimensions, (ii) scattering mechanisms, (iii) temperature, and (iv) doping type and concentration in the case of semiconducting interconnects. Physical models of electron diffusion coefficient in the presence of size effects in various interconnect materials are developed in Chapter V.

The energy dissipation of the spin-diffusion interconnect is given by the joule heating that occurs along the path of the electric current flow. In Figure 14, electric current flows between FM-1 and FM-2 through the non-magnetic channel of length L_1. The energy dissipation of the spin-diffusion interconnect is mathematically given

Table 3: Diffusion coefficient of electrons in various materials that can serve as the interconnect in the spin-valve circuits. Values are provided at 300K. W/T is the width-to-thickness ratio of the films used in experiments. In the case of graphene, only the width is given. N_d denotes the n-type dopant concentration in semiconducting interconnects.

Material	**Diffusivity** (cm^2/s)	**W/T**	**Reference**
Copper	80	100nm/54nm	[69]
Aluminum	120	150nm/50nm	[93]
Silicon ($N_d = 1.8 \times 10^{19} 1/cm^3$)	3.7	bulk	[40]
Gallium Arsenide (low doping)	≤ 200	bulk	[132]
Graphene	160	W = 300nm	[99]

as

$$E_{DIFF,spin} = I_{elec}^2 R_{tx} \Delta t, \tag{11}$$

where R_{tx} is the resistance of the transmitter side, and Δt is the pulse width of the electric current. The pulse width of the electric current must be greater than the delay of the interconnect between the driver and the receiver. This condition ensures that the information-bearing spin signal reaches the receiver nanomagnet FM-3 before the input signal toggles. The transmitter resistance consists of the resistance of the nanomagnets FM-1 and FM-2 (R_{FM1} & R_{FM2}), the resistance of the interconnect between FM-1 and FM-2 (R_{int,L_1}), the tunnel barriers between the nanomagnets and the interconnect (R_{c1} & R_{c2}). In the case of graphene, quantum resistance (R_Q) at the contacts also needs to be taken into account. Hence, R_{tx} is mathematically given as

$$R_{tx} = R_{FM1} + R_{FM2} + (R_{c1} + R_{c2} + R_{int,L1} + R_Q)/N_{ch}, \tag{12}$$

where N_{ch} is the number of conduction channels in the graphene interconnect. In the case of graphene, R_{int,L_1} is given as

$$R_{int,L1} = R_Q \frac{L_1}{\lambda}, \tag{13}$$

where λ is the mean free path of carriers in graphene. In a good-quality graphene sample, λ may be as large as 1 μm [156].

Thermal diffusion interconnects: "Thermal-logic gates" in which phonons are used for information processing have been discussed in literature [131]. It has been shown that phonons, the carriers of heat, can carry information and may pave the way for the next-generation phononic computer in analogy with an electronic computer. Recently, graphene thermal transistor has been discussed by Wang et al [131]. Thus, in theory, there is a possibility to build a physical system that uses temperature as the state variable. Graphene and/or carbon nanotubes may serve as the material for fabricating such a device. Also, interconnects in this system can be fabricated from the same material providing an all-graphene or an all-carbon-nanotubes system and will overcome the problem associated with hybrid integration of different technologies [131]. To carry information in phonon-based systems, diffusion interconnects can be used. We seek the solution of the one-dimensional isothermal heat equation to obtain the delay of the thermal interconnects. The diffusion equation for phonon logic is better known as the "heat equation". The temperature-dependent heat equation is given as

$$\rho c(T)\frac{\partial T}{\partial t} = \frac{\partial}{\partial x}\left(\kappa(T)\frac{\partial T}{\partial x}\right), \tag{14}$$

where ρ is the mass density of the material Kg/m^3, $c(T)$ is the temperature-dependent heat capacity in $J/Kg.K$, and $\kappa(T)$ is the thermal conductivity in $W/m.K$. The temperature-dependent specific heat capacity, $c(T)$, and thermal conductivity, $\kappa(T)$, of a (15,15) armchair single-walled carbon nanotubes (SWNT) are given as [81]

$$c(T)\{J/Kg.K\} = 2.5642T - 61.7294, \tag{15a}$$

$$\kappa(T)\{W/m.K\} = \frac{1}{3.7\times10^{-7}T + 9.7\times10^{-10}T^2 + 9.3\,(1+0.5/L)\,T^{-2}}, \tag{15b}$$

where T is the temperature in K, and L is the interconnect length. The temperature range of validity of Eqs. (15a) and (15b) is from 250K to 350K. The time-dependent solution of the heat equation is obtained under the following boundary conditions:

$$T(x, t=0) = T_L, \tag{16a}$$

$$T(x=0,t) = (T_H - T_L)\left(\frac{t}{t_r}u\left(1-\frac{t}{t_r}\right) + u\left(\frac{t}{t_r}-1\right)\right) + T_L, \tag{16b}$$

$$\frac{\partial T}{\partial x}(x=L,t) = 0, \tag{16c}$$

where T_L is the temperature of the interconnect at time t=0, T_H is the steady-state temperature of the interconnect, and t_r is the rise time of the input signal at x=0, and $u(.)$ is the step function. T_L and T_H may be used to represent digital logic levels of "0" and "1" or vice-versa. Figure 16 shows the time-dependent solution of Eq. (14) using the boundary conditions in Eqs. (16a)-(16c) for two cases. In Case (i), a temperature-independent thermal diffusivity, k_{th}, is considered by using values of $c(T)$ and $\kappa(T)$ at T=300K. In this case, the thermal diffusivity is defined as

$$k_{th} = \frac{\kappa(T=300K)}{c(T=300K)\rho}, \tag{17}$$

where ρ is the material density of carbon nanotubes. Case (ii) considers temperature-dependent models of both $c(T)$ and $\kappa(T)$ as in Eqs. (15a) and (15b), respectively.

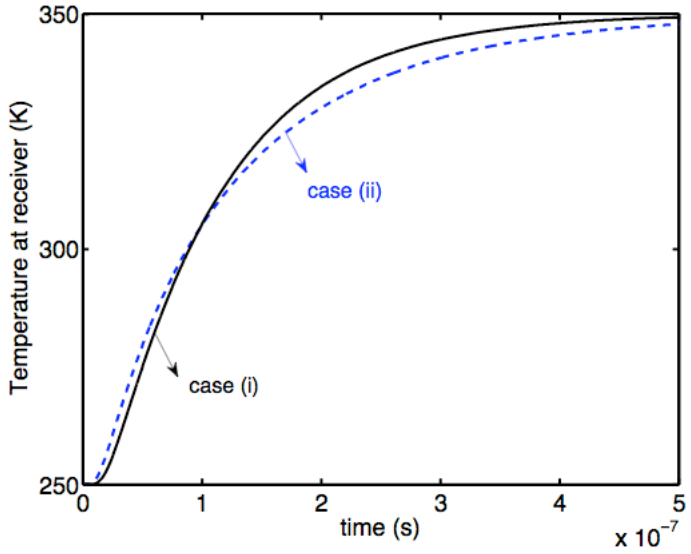

Figure 16: Temperature at the receiver as a function of time for case (i) when thermal diffusivity is assumed to be constant (at 300K), and case (ii) when temperature dependent models are used.

From Figure 16, it can be seen that the effect of having temperature-dependent conductivity and specific heat capacity have only a minor impact on the overall time constant of the temperature to reach its steady state. Thus, using isothermal heat equation is justified, especially since it would be preferred to transmit information via phonons with minimum temperature difference along the interconnect to minimize the energy dissipation of the interconnect. Hence, the 50% time delay of the signal for phonon-diffusion interconnects is given as

$$t_{DIFF,phonon} = \gamma_{th} \frac{L^2}{k_{th}}, \tag{18}$$

where γ_{th} is the constant of proportionality and depends on the rise time of the signal. Figure 17 shows γ_{th} versus the signal rise time. For an infinitesimally small rise time, $\gamma_{th} \approx 0.38$.

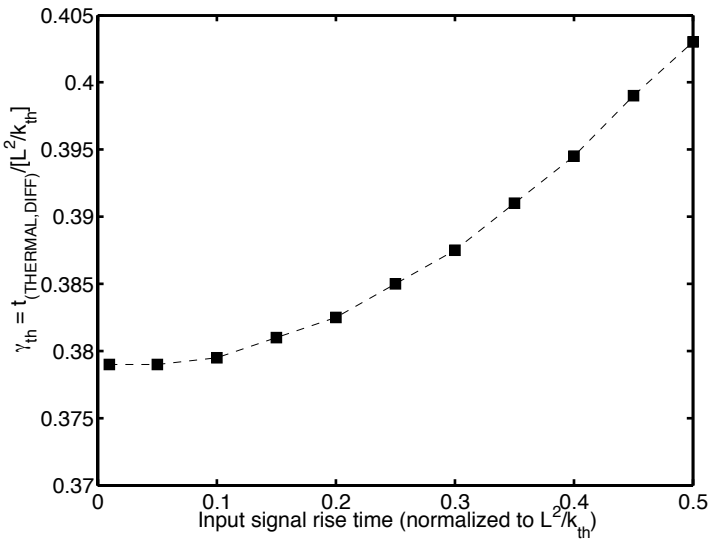

Figure 17: The 50% delay of phonon-diffusion interconnects as a function of the rise time of the input signal.

The energy dissipation of phonon-diffusion interconnects is given by the amount of energy needed to raise the temperature of the interconnect from its initial value to

its final steady-sate value. This is mathematically expressed as

$$E_{DIFF,thermal} = \int_{T_L}^{T_H} mc(T)dT, \tag{19}$$

where m is the mass of the interconnect. Using an average value of the specific heat capacity at $T = (T_H + T_L)/2$, the energy dissipation, $E_{DIFF,thermal}$ can be simplified to

$$E_{DIFF,thermal} = mc'\Delta T, \tag{20}$$

where $\Delta T = (T_H - T_L)$, and c' is the average value of the specific heat capacity of the interconnect material. In terms of the interconnect length, $E_{DIFF,thermal}$ can be expressed as

$$E_{DIFF,thermal} = \pi(Di)b\rho c'(\Delta T)L, \tag{21}$$

where Di is the SWNT diameter, b is the SWNT thickness, and ρ is the material density of SWNT. To reduce the energy dissipation of phonon-diffusion interconnects (i) interconnect material with a lower specific heat capacity must be used and/or (ii) ΔT must be reduced. Specific heat capacity is analogous to the interconnect capacitance for conventional CMOS interconnects; ΔT is analogous to the supply voltage, V_{DD}, in electrical interconnects.

2.2.1.2 Drift interconnects

Drift interconnects use an external electric field to manipulate carriers that have a net charge associated with them. Drift is a possible transport option for an all-spin transistor since spin is a quantum-mechanical property of an electron. Since an electron by virtue of its charge moves with drift velocity upon application of an external electric field, electron spin may be transported by drift as well. Drift can also be used for transporting indirect excitons. An indirect exciton consists of spatially separated electron and hole pairs as in bilayer graphene [211], [50]. Drift interconnects may be faster for systems in which the electron drift speed is greater than its diffusion

speed. A conventional spin valve that uses drift to transmit information encoded in the electron spin is shown in Figure 18. In this circuit, the electric and the spin currents flow along the same path. The transmitting nanomagnet is labelled as FM-1 and the receiving nanomagnet is labelled as FM-2. The equivalent circuit diagram of the drift interconnect is also shown in Figure 18. A current source is connected between the two terminals FM-1 and FM-2. The transmitter side of the circuit includes a high-resistance barrier to increase the spin-injection efficiency. At the receiver side, there is an ohmic contact between the nanomagnet and the interconnect to minimize the back-injection of carriers. The transmitter and the receiver sides are separated from each other by an isolator, which is typically an oxide barrier to prevent mixing of carriers. The circuit does not include capacitance or inductance of the interconnect since the aim is to obtain an upper bound on the speed and the energy dissipation of drift interconnects.

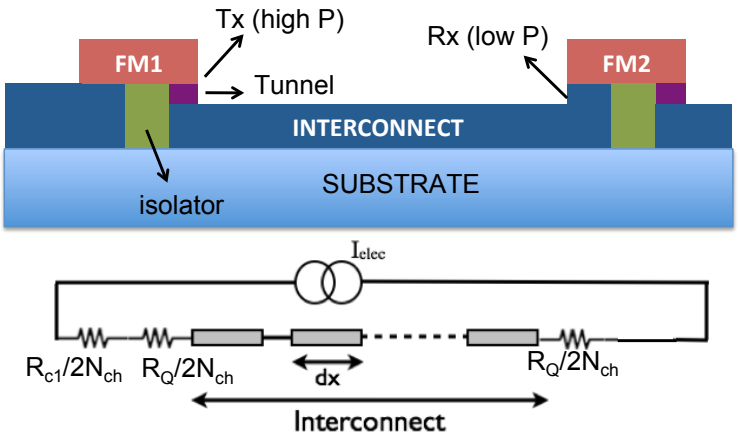

Figure 18: (top) A conventional spin valve that uses drift transport of electron spins between the driver and the receiver. (bottom) The equivalent circuit diagram of the drift interconnect.

The delay associated with drift interconnects is given as

$$t_{DRIFT} = \frac{L}{v_d}, \tag{22}$$

where v_d is the drift velocity of carriers in the interconnect. The drift velocity of

electrons in the interconnect can be obtained by first calculating the actual electric field across the interconnect length. When the interconnect length is comparable to the mean free path of electrons, the effect of quantum resistance cannot be ignored. At low electric fields, the resistance per unit length of the interconnect is only dependent on the low-field mean free path of electrons in the interconnect. The drift velocity, v_d, of electrons is given as $\mu_0 E_{net}$, where μ_0 is the mobility of electrons in a long interconnect, and E_{net} is the net electric field across the interconnect. The mobility of electrons in a high-quality graphene sample may be as high as 10,000 cm^2/Vs [22]. The net electric field across the graphene interconnect is given as

$$E_{net} = \frac{\Delta V - I_{elec}\left(R_Q + R_c\right)/N_{ch}}{L}, \tag{23a}$$

$$\Delta V = I_{elec}\left(\frac{R_Q + R_Q L/\lambda + R_c}{N_{ch}}\right), \tag{23b}$$

where ΔV is the voltage difference across the interconnect, λ is the mean free path of electrons in the interconnect at low electric fields. Using Eqs. (23a) and (23b), the net electric field across the interconnect and the drift velocity are expressed as

$$E_{net} = I_{elec}\frac{R_Q}{N_{ch}\lambda}, \tag{24a}$$

$$v_d = \frac{\mu_0 I_{elec} R_Q}{N_{ch}\lambda}. \tag{24b}$$

Using v_d from Eq. (24b), the delay of the drift interconnect is given as

$$t_{DRIFT} = \frac{L\lambda N_{ch}}{\mu_0 I_{elec} R_Q}. \tag{25}$$

The drift-based interconnect for particle transport is significantly different from the CMOS interconnect, which is an RC-based interconnect. In an RC interconnect, information is transmitted through a voltage wave that diffuses from the driver to the receiver [11]. Although the nature of the voltage-diffusion equation is similar to the particle-diffusion equation, the speed at which information can travel in an

RC interconnect is much higher than the speed at which particles are physically transported through the interconnect.

The energy dissipation of the spin-drift interconnects is given as the product of the joule heating term, $I_{elec}^2 R$, and the pulse width of the electric current, which may be set equal to the delay of drift interconnects. Mathematically, the energy dissipation of spin-drift interconnects is given as

$$E_{DRIFT} = I_{elec}^2 R \Delta t, \tag{26}$$

where R is the resistance of the spin-valve circuit shown in Figure 18, and $\Delta t = t_{DRIFT}$. The resistance of the circuit, R, is given as

$$R = R_{FM1} + R_{FM2} + \frac{R_c + R_Q + R_Q L/\lambda}{N_{ch}}. \tag{27}$$

Using Eqs. (25)-(27), the energy dissipation of drift interconnects is expressed as

$$E_{DRIFT} = \frac{I_{elec} L \lambda}{\mu_0} \left(\frac{R_{FM1} + R_{FM2}}{R_Q / N_{ch}} + \frac{R_c}{R_Q} + \left(1 + \frac{L}{\lambda} \right) \right). \tag{28}$$

2.2.1.3 Ballistic interconnects

Ballistic transport refers to the movement of carriers without scattering events in a medium. Ballistic transport is typically observed in low-dimensional conductors because of their limited phase space for carrier scattering. Ballistic transport of electron spins can occur without any net-charge transport, thereby yielding pure-spin current and zero electric current. If the number of right-mover electrons is equal to the number of left-mover electrons in the ballistic channel between the driver and the receiver, then the net electric current in the channel is zero. However, if the spin polarization of carriers in the left reservoir (driver) is different than the spin polarization of carriers in the right reservoir (receiver), then a pure spin current can flow from the driver to the receiver (see Figure 19). In graphene, the E-K relationship near the Dirac point can be modeled as a linear relationship (see Figure 19); this makes

the velocity of carriers independent of their energy and equal to the Fermi velocity, $v_f = 8 \times 10^5 m/s$. Hence, electron spins in graphene may be communicated at their Fermi velocity. The ballistic nature of the conductor prevents any collisions between the left- and right-mover electrons. The delay of a ballistic interconnect is given as

$$t_{BALL} = \frac{L}{v_f}. \tag{29}$$

If the interconnect is longer than the mean free path of the carriers in the interconnect, ballistic transport will tend towards a diffusive transport; in this case, a unified ballistic-diffusive transport model is necessitated. The steady-state flux of the carriers in quasi-ballistic regime is given as

$$J_s = \frac{D}{L} \frac{s(0)}{1 + \frac{D}{L}\frac{1}{v_f}}, \tag{30}$$

where $s(0)$ is the steady-state carrier concentration in $1/cm$ at the beginning of the interconnect, D is the diffusivity of carriers in the interconnect in cm^2/s, and L is the interconnect length in cm, v_f is the Fermi velocity of carriers in the interconnect in cm/s. In the ballistic limit, J_s converges to $s(0)v_f$; in the diffusive limit, J_s converges to $s(0)\frac{D}{L}$. The steady-state carrier concentration, $s(z)$, in the interconnect is given by a linear profile as

$$s(z) = s(0)\left(1 - \frac{z}{L}\right) + \frac{s(L)}{L}. \tag{31}$$

The transit time of the carriers through the interconnect is given as

$$t_{tr} = \frac{\int_0^L s(z)}{J_s}. \tag{32}$$

Using Eqs. (31) and (32), the transit time of carriers in the quasi-ballistic interconnect is simplified to give

$$t_{QUASI-BALL} = \frac{L^2}{2D} + \frac{L}{v_f}. \tag{33}$$

However, since the aim is to compare the best-case performance of various novel interconnects, a model corresponding to pure ballistic transport is sufficient for this

analysis. In addition to spins, phonons in graphene can also be transported ballistically. The delay for phonon-ballistic interconnect is the same as in Eq. (29) with v_f replaced with the speed of phonons in graphene, v_{ph}. Hence, the delay of phonon-ballistic interconnects is given as

$$t_{BALL,thermal} = \frac{L}{v_{ph}}. \tag{34}$$

In graphene, the speed of acoustic phonons is equal to 20Km/s [159].

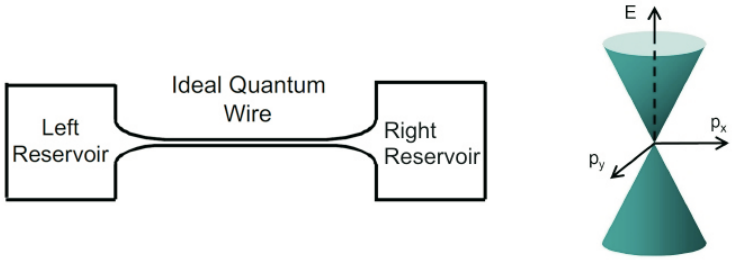

Figure 19: An ideal quantum wire is shown on the left. The energy dispersion relation of graphene is shown on the right. Electron charge current is zero if the number of left-mover and right-mover electrons is same. However, the net spin current can be non-zero if the spin polarization in the left reservoir is changed.

Assuming electrical injection of electron spins in the ballistic interconnect, the energy dissipation of spin-ballisitic interconnects is given as

$$E_{BALL,spin} = I_{elec}^2 R_{tx} \frac{L}{v_f}, \tag{35}$$

where R_{tx} is given in Eq. (12).

2.2.2 Wave-based interconnects

In wave-based interconnects, communication of information is supported in a wave-based fashion without the actual movement of particles. Amongst the wave-based interconnects, optical interconnects that carry information via electromagnetic waves are the most popular. Even though optical interconnects possess large data-carrying capabilities, they are not discussed in this research. This is because the implementation of optical interconnects at the nanoscale level is hampered because of the size

mismatch between the electronic and the photonic components on the microprocessor. There is at least an order of magnitude size mismatch between the electronic and the photonic components in which the transverse dimensions of components are limited to $\approx \lambda/2$, where λ is the wavelength of light used for encoding information [168]. The wave-based interconnects considered in this research are: (i) spin-wave-bus interconnects and (ii) plasmonic interconnects.

2.2.2.1 Spin-wave-bus interconnects

A spin wave is a collection of precession of electron magnetic moment about a magnetic field. Spin waveguides can be made of magnetic films, a wire, or a combination of wires made of ferromagnetic (FM) films, anti-ferromagnetic materials, or ferrite materials [106]. Figure 20 shows a typical spin-wave-bus circuit with an FM film such as CoFe used for carrying spin waves between the asymmetric coplanar strip (ACPS) transmission lines that serve to excite and detect spin waves. Information in a spin-wave-bus circuit is encoded in the phase of the spin wave. Phases of "0" and "π" may be used to represent logic states "1" and "0" or vice-versa. The polarity of the inductive voltage generated at the receiver is used for detecting the signal. The propagation speed of spin waves depends on factors such as the waveguide material and structure, spin-wave frequency and the magnitude and direction of the external magnetic field. The delay of spin-wave interconnects can be given as L/v_{SWB}, where v_{SWB} is the propagation velocity of spin waves in the material. The highest reported velocity of magnetostatic propagation mode of spin waves is 10^5 m/s in materials with a high Curie temperature such as Co and Fe. The propagation velocity of spin waves continually decreases at higher frequencies [109].

The energy dissipation of the spin-wave-bus interconnect is given by the amount of energy needed by an external magnetic field to create a magnetization change equal to the amplitude of the spin wave in the ferromagnetic film of a given volume [108].

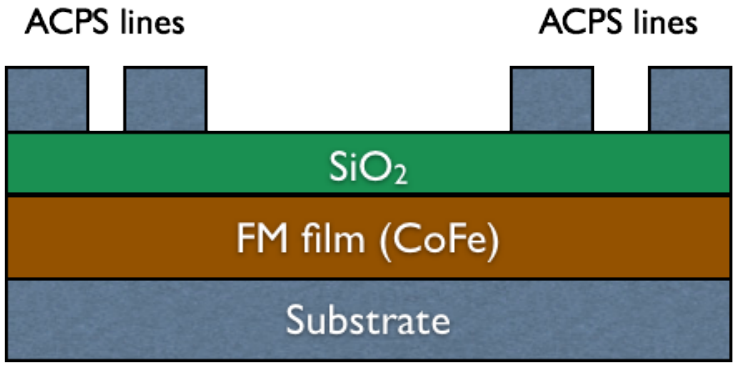

Figure 20: A spin-wave-bus circuit with CoFe ferromagnetic film used as the conduit of spin information. The asymmetric coplanar strip transmission lines on the top of the structure are used to excite and detect spin waves. Figure adapted from [108].

Mathematically, the energy dissipation associated with the transmission of spin waves through the interconnect is given as

$$E_{SWB} = \mu_0 \Delta M H_{ext} V, \tag{36}$$

where μ_0 is the free-space permeability, ΔM in A/m is the change in magnetization of the spin waveguide upon application of an external magnetic field, H_{ext}, in A/m, and V is the volume of the interconnect. Although the intrinsic energy dissipation of spin wave interconnects may be as low as few tens of thermal energy, $k_B T$, the energy needed to excite spin waves may be significantly higher. The excitation energy is given as

$$E_{ext,SWB} = I_{ext}^2 \tau_{ext} Z, \tag{37}$$

where I_{ext} is the excitation current, τ_{ext} is the time duration of the excitation pulse, and Z is the impedance of the microstrip antenna used to excite spin waves. The excitation energy can be eight or nine orders of magnitude higher than the thermal energy [108].

2.2.2.2 Plasmonic interconnects

Plasmonics refers to the technology of transporting light energy in matter structures that are of smaller dimensions than the corresponding wavelength of light used for encoding information. The conduit for propagation of plasmons is termed as the plasmon waveguide and can be implemented in a variety of ways [178]. Plasmonic stripe waveguides (resembling conventional metal interconnects) or metal nanoparticles embedded in a dielectric may serve as the propagation medium for plasmons. The delay of plasmonic interconnects can be expressed as $t_{plasmonic} = (\gamma_p/c)\, L$, where L is the plasmonic interconnect length, c/γ_p is the speed of propagation of the plasmon in the waveguide. The factor γ_p depends on the frequency of plasmon, the waveguide material, and the waveguide structure. Numerical simulations of cylindrical Ag plasmonic waveguides embedded in SiO_2 were conducted by Conway et al. [37] to obtain the factor γ_p for different sizes of waveguides and at different free-space wavelengths. These values are provided in Table 4.

Table 4: Data from Conway & coworkers, 2007 [37] of group velocity of cylindrical Ag plasmonic interconnects in SiO_2 dielectric. λ^{free} is the free-space wavelength, v_g is the group velocity of the plasmons, c_0 is the speed of light in vacuum, and $1/\alpha$ is the propagation length of the plasmons.

Diameter (nm)	λ^{free} **(nm)**	v_g/c_0	$1/\alpha$ **(μm)**
10	500	0.02	<<1
10	1000	0.1	0.5
50	500	0.12	<<1
50	1000	0.38	3

The energy dissipation of plasmonic interconnects depends on the number of plasmons needed per bit of information. If the digital logic state "1" is represented by a collection of m plasmons, and the digital logic state "0" is represented by zero plasmons, then a mean number of $m/2$ plasmons are needed in an unbiased channel to transmit information. The average number of plasmons can be calculated from

the shot noise limited transmission of plasmons for a given bit error rate (BER). The mean number of plasmons needed to encode one bit of information for a BER of 10^{30} is equal to 34 [37]. However, due to the loss in signal strength as plasmons propagate through the interconnect, the minimum energy transmitted per bit (assuming unity quantum efficiency) is given as

$$E_{plasmon} = \frac{1}{2} m \hbar \omega e^{\alpha L}, \tag{38}$$

where ω is the operating frequency, and $1/\alpha$ is the propagation length of plasmons. The propagation length of plasmons is defined as the characteristic length at which the intensity of plasmons decays to $1/e$ times its initial value, where e is the Neperian number. Table 4 shows the value of $1/\alpha$ for different diameters of Ag cylindrical waveguide in SiO_2 simulated by Conway et al. using COMSOL [37]. COMSOL Multiphysics (previously known as FEMLAB) is an interactive environment for modeling and solving scientific and engineering problems based on PDEs.

As seen from Table 4, the attenuation of plasmons is weak at long wavelengths and large diameter wires, where plasmon confinement is weak and much of the plasmon energy lies in the relatively loss-free dielectric.

2.3 Comparison of Novel and CMOS Interconnects

The performance and the energy dissipation of novel and CMOS interconnects are compared at the end of the silicon-technology roadmap (minimum feature size of 7.5nm). The limitations imposed by interconnects on novel circuits are identified. In order for novel interconnects to be as fast as CMOS interconnects, it is shown that interconnects in novel circuits have to be shorter in length. The concept of "area scaling" is developed.

2.3.1 Particle-based interconnects versus CMOS interconnects

The delay of particle-transport interconnects versus interconnect length in gate pitches is plotted in Figure 21 at the ITRS technology year of 2024. Assuming an average of four transistors per logic gate, the gate pitch from ITRS projections is found to be 140 nm at the 2024 ITRS technology year [1]. For novel interconnects, only the intrinsic interconnect delay is plotted and the non-idealities imposed by novel switches are not considered. This assumption is made to derive an upper bound on the performance of novel interconnects. Also plotted in Figure 21 is the CMOS interconnect delay. Two driver sizes for the CMOS interconnect are considered: channel width-to-length ratio (i) W/L = 1 and (ii) W/L = 5 (also termed "5×"). In high-performance logic, minimum-sized drivers are rarely used because of their limited drive capability. The material parameter values to evaluate the performance of particle-based interconnects are tabulated in Table 5.

Table 5: Material parameters to evaluate the performance of particle-transport interconnects. Thermal conductivity, κ, and specific heat capacity, c, are quoted at 300K for single-walled carbon nanotubes. Thermal properties of carbon nanotubes are strong functions of temperature and also depend on their size quantization. These values are only representative values used for comparing thermal interconnects with other interconnects. κ and c in graphene-based interconnects are also quite similar.

Parameter	Value	Reference
Electron diffusion coefficient	200 cm^2/s	N. Tombros et al., 2007 [223]
Electron mobility	28,000 cm^2/Vs	N. Tombros et al., 2007 [223]
Thermal conductivity	2400 $W/m.K$	D. Nika, 2009 [159]
Specific heat capacity	800 $J/Kg.K$	J. Hone, 2008 [83]
Material density	1300 Kg/m^3	
Electron mean free path	1.2 μm	A. Naeemi and J.D. Meindl [154]
Velocity of sound	20 Km/s	D. Nika et al., 2009 [159]

Except for spin-ballistic interconnects, the delay of novel interconnects discussed here is larger compared to CMOS interconnects. This means that even if the new technology were to employ perfect switches with negligible delays, the new circuits

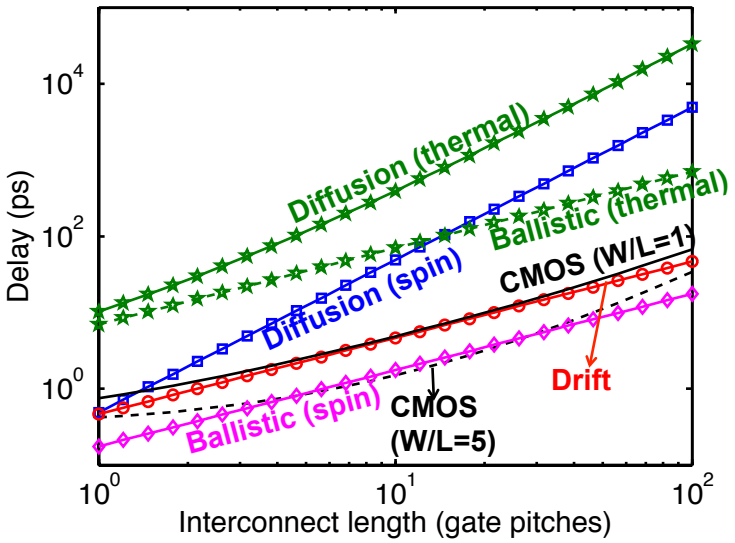

Figure 21: Delay versus interconnect length for particle-transport interconnects as a function of interconnect length in gate pitches. The delay of CMOS interconnects for two driver sizes (W/L=1 and W/L=5) is also plotted at the 2024 technology node.

will be slower owing to the slow transport through the interconnects. Diffusion interconnects with a diffusion coefficient of 200 cm^2/s are slower compared to CMOS interconnects. Figure 22 shows the minimum required electron diffusion coefficient in order for spin-diffusion interconnects to be equally fast as the CMOS interconnects. Point "a" in Figure 22 shows that an electron diffusivity of 2000 cm^2/s is required for spin-diffusion interconnects of length 10 gate pitches to have the same delay as CMOS interconnects driven by minimum-sized driver. This value of electron diffusion coefficient is more than an order of magnitude larger than the experimentally reported value of diffusion coefficient in graphene [223]. At point "b" in Figure 22, the minimum required diffusivity is 7000 cm^2/s, which may be quite challenging to achieve even in high-mobility graphene.

Owing to the extremely small thermal diffusivity for phonons, diffusion interconnects for phonons have the maximum delay, which is more than an order of magnitude

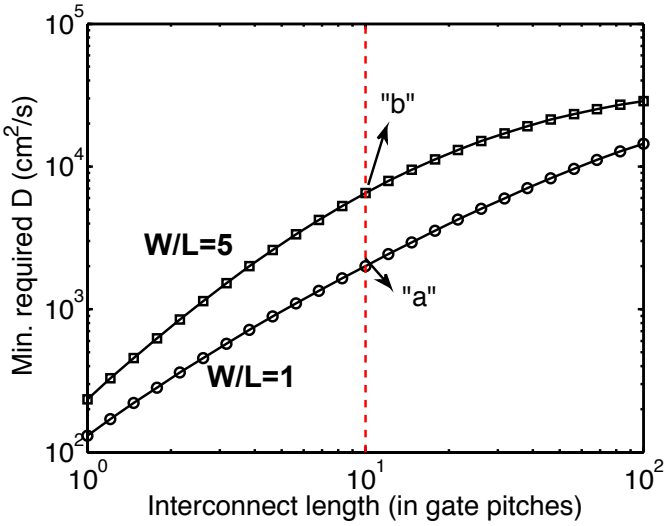

Figure 22: Minimum required diffusion coefficient, D, in spin-diffusion interconnects to achieve an equal performance as the CMOS system at the 2024 technology node. The value of diffusion coefficient required at 10 gate pitches for spin-diffusion interconnects to be able to match in performance with CMOS interconnects is 2000 cm^2/s (point "a") and 7000 cm^2/s (point "b") for CMOS interconnect driven by minimum-sized driver and 5× driver, respectively.

larger than the delay of CMOS interconnects as short as one gate pitch. Also phonon-ballistic interconnects are slower than CMOS interconnects since the speed of phonons in graphene is around 20 Km/s. Spin-drift interconnects with $I_{elec} = 10\ \mu A$, $\mu_0 = 10^4\ cm^2/Vs$, and $\lambda = 1\ \mu m$ are faster than diffusion interconnects but slower than CMOS interconnects. Ballistic interconnects are faster than CMOS interconnects driven by minimum-sized CMOS drivers. However, spin-ballistic interconnects are only slightly slower compared to CMOS interconnects driven by a 5× CMOS driver if the interconnect is longer than four gate pitches.

To obtain equal performance in post-CMOS logic, interconnects in emerging logic have to be shorter. This can be achieved if new switches are made smaller than Si FETs and/or fewer gates are needed to do the same task; both of these factors scale down circuit area and hence interconnect length.

One can derive the area-scaling factor needed in the new logic to achieve an equal

performance as the CMOS logic. This is obtained by equating the delays of the novel and CMOS interconnects. The area-scaling factors obtained for novel technologies do not take device delays into account and, therefore, denote only optimistic values of area-scaling factors. The required area-scaling factors would be more severe if intrinsic device delays were taken into account. Assuming that the gate pitch in the new logic is scaled by a factor of $L_{p,CMOS}/L_{p,newlogic}$ (L_p is the gate pitch) and that the number of gates needed to implement a logic function is scaled by $N_{CMOS}/N_{newlogic}$, one can obtain the area-scaling factor of the new logic as

$$AS = \frac{A_{CMOS}}{A_{newlogic}} = \frac{N_{CMOS}}{N_{newlogic}} \times \left(\frac{L_{p,CMOS}}{L_{p,newlogic}} \right)^2 \tag{39}$$

Figure 23 shows the area-scaling factor versus interconnect length when the CMOS interconnect is driven by a minimum-sized CMOS driver. From this figure, it can be seen that the required area-scaling factor for ballistic interconnects is the lowest. This means that for spin-ballistic interconnects a larger circuit area may be tolerated without any delay penalty. Diffusion and ballistic interconnects for temperature as the state variable are considerably slower than the CMOS interconnects; therefore, the area-scaling factor required of them is the largest amongst all the particle-based interconnects. The required area-scaling factor increases with interconnect length for spin-diffusion and phonon-diffusion interconnects. However, for drift and ballistic interconnects the required area-scaling factor increases with interconnect length for short interconnects and then begins to decrease for longer interconnects. This behavior of area-scaling factor with interconnect length for ballistic and drift interconnects results from the fact that the delay of CMOS interconnects increases more rapidly with increasing interconnect length as compared to the delays of ballistic and drift interconnects. For longer interconnects, the delay of CMOS interconnects shows a super-linear dependence on the interconnect length, while the delay of perfectly ballistic and drift interconnects increases only linearly with interconnect length.

Table 6 gives the area-scaling factors for various novel interconnects to match in

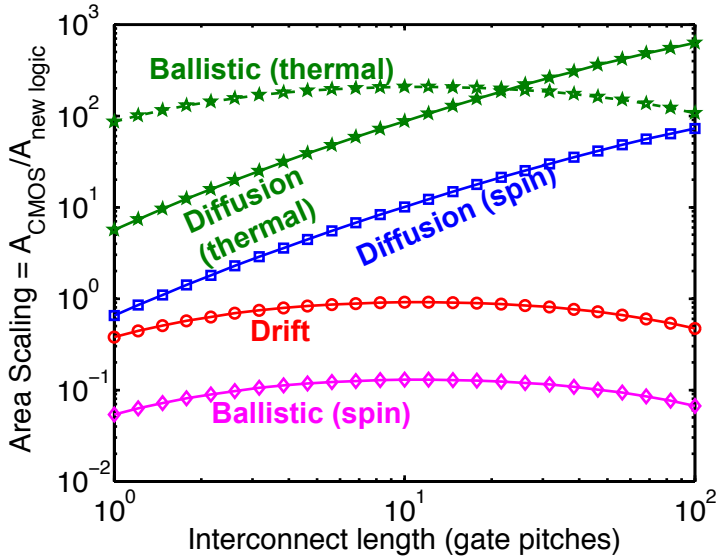

Figure 23: Area-scaling (AS) factors of various particle-based novel interconnects versus interconnect length in gate pitches. The CMOS driver size is W/L=1.

performance when compared with the CMOS system at the minimum and 5× driver sizes. Area-scaling factors for various interconnects are tabulated for an interconnect that is 10 gate pitches long. The size of the CMOS driver has a significant impact on the area-scaling factors required for the new logic to match the performance of the CMOS system. The area-scaling factors for most novel interconnects are much greater than unity. Such large area-scaling factors may be very demanding for the new logic technology. This may mean that the new circuits may operate at a lower speed. To mask the delay of interconnects in the new logic, smart architectures that favor parallel processing are highly desired. Apart from the speed limitations, there may be other factors which may limit the potential use of interconnects discussed here. For example, in the case of ballistic interconnects, it is required that the mean free path of the electron be long enough to support ballistic transport of information at all interconnect lengths. Further, the spin-flip length of the electrons, in the case of spin interconnects, must be large enough to avoid significant decay in concentration as the electrons move through the interconnect.

Table 6: Area-scaling factors of various particle-based interconnects to match in performance with CMOS interconnects. W/L denotes the width-to-length ratio of the CMOS driver. The values in the table are obtained for an interconnect of length 10 gate pitches.

Interconnect Type	**W/L=1**	**W/L=5**
Spin diffusion	10.7	32.5
Spin ballistic	0.13	1.35
Spin drift	0.91	9.56
Thermal diffusion	87.5	283.5
Thermal ballistic	206.6	2162.3

The energy dissipation of particle-based interconnects is plotted in Figure 24. For reference, the energy dissipation, $1/2CV^2$, of the CMOS system is also plotted at the 2024 technology node. Energy dissipation of spin diffusion, drift, and ballistic interconnects is plotted for perfect spin-injection efficiency to obtain a lower bound on their energy dissipation. The number of conduction channels for spin interconnects implemented with graphene is assumed to be unity. The energy dissipation of ballistic interconnects is lowest among all particle-based interconnects. This is because the pulse width of the electric current used for spin injection is much lower in the case of ballistic interconnects owing to the high Fermi velocity of electrons in graphene. Spin-diffusion interconnects have a lower energy dissipation compared to CMOS interconnects for interconnect lengths up to seven gate pitches. Spin-drift interconnects are more energy efficient compared to CMOS interconnects for interconnect lengths up to 55 gate pitches. Spin-drift interconnects are also more energy efficient compared to spin-diffusion interconnects for interconnects longer than one gate pitch. This is because of the lower drift-interconnect delay, which reduces the requirement on the pulse width of the electrical current, and thereby helps to lower the ohmic energy dissipation of drift interconnects. Phonon-diffusion interconnects have a lower energy dissipation compared to CMOS interconnects but consume more energy relative to ballistic interconnects.

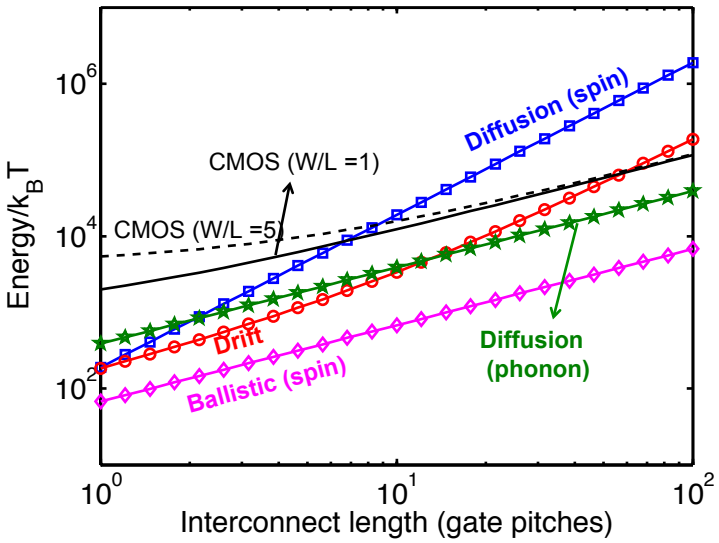

Figure 24: Energy dissipation of particle-based interconnects versus interconnect length in gate pitches. Also plotted is the energy dissipation of CMOS interconnects at the 2024 technology year.

2.3.2 Wave-based interconnects versus CMOS interconnects

The delay associated with wave-based interconnects is plotted as a function of the interconnect length in Figure 25. The delay associated with switches in the new technology is again neglected to establish an upper bound on the performance of novel interconnects. It can be seen from Figure 25 that plasmonic interconnects are orders of magnitude faster compared to CMOS interconnects as well as other novel interconnects. This is because the propagation speed of plasmons can be comparable to the speed of light in the dielectric medium of the plasmon waveguide.

The delay through the spin-wave-bus interconnects is plotted for propagation speeds of 10^4m/s (realistic value) and 10^5m/s (optimistic value). It can be seen from Figure 25 that spin-wave-bus interconnects are always slower compared to CMOS interconnects. To obtain an equal performance as CMOS interconnects, circuits utilizing spin-wave bus interconnects must be made smaller in area.

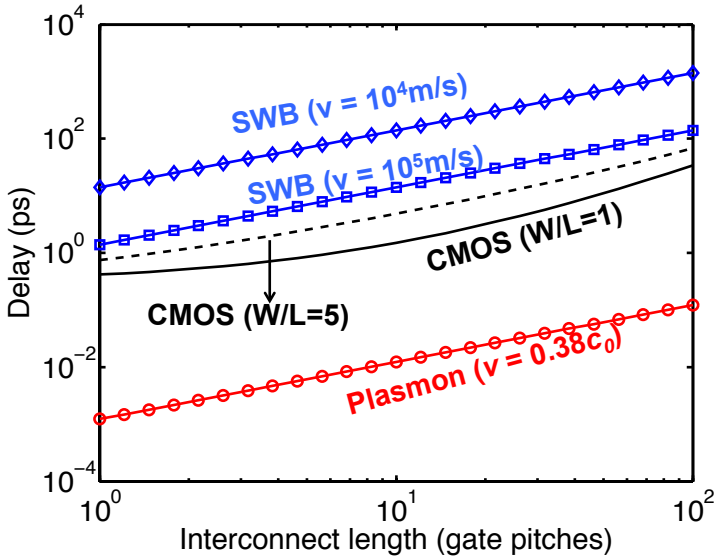

Figure 25: Delay versus interconnect length for wave-based interconnects.

The required area-scaling factor for spin-wave-bus interconnects is plotted in Figure 26. When compared with CMOS interconnects driven by minimum-sized drivers, an area-scaling factor of $\approx 8\times$ is required for spin-wave-bus interconnects having a propagation speed of 10^5 m/s, while an area-scaling factor of approximately $800\times$ is required for spin-wave-bus interconnects having a propagation velocity of 10^4 m/s at a CMOS-interconnect length of 10 gate pitches. The required area-scaling factor shoots up by $10\times$ when spin-wave-bus interconnects are compared with CMOS interconnects driven by $5\times$ drivers. Such large area-scaling factors are quite challenging for spin-wave-bus circuits. In addition, the scalability of spin-wave-bus interconnects below the spin wavelength poses a significant challenge [105]. While the width and the thickness of a spin-wave-bus interconnect can be scaled down to several nanometers, to make the interconnect length shorter, the wavelength must be reduced. A representative value of the spin wavelength based on defect tolerance is estimated to be 100 nm [105]. Hence, the concept of scaling the footprint of the device to shorten the interconnect length may not be viable in spin-wave-bus circuits.

The energy dissipation of wave-based interconnects as a function of interconnect

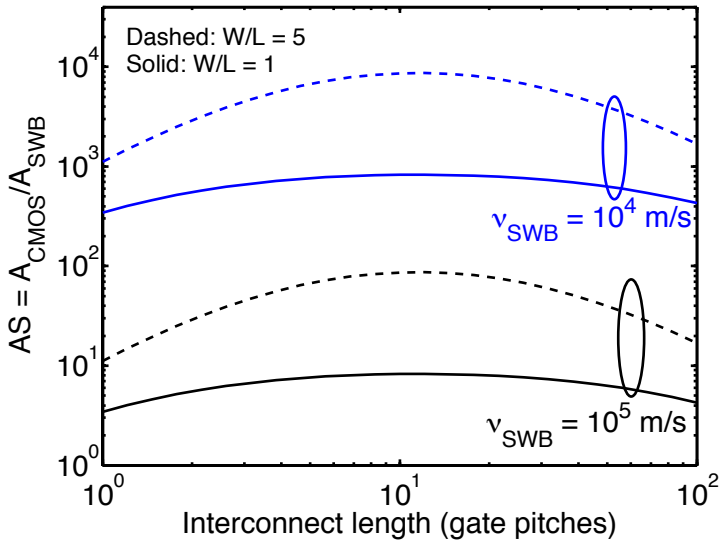

Figure 26: Area scaling versus interconnect length in gate pitches for spin-wave-bus interconnects. Two wave velocities are considered: (i) $\nu_{SWB} = 10^4$m/s (realistic) and (ii)$\nu_{SWB} = 10^5$m/s (optimistic). Two driver sizes for CMOS interconnects are also considered: (i) W/L = 1(minimum-sized driver) and (ii) W/L = 5 (5× the minimum-sized driver).

length is plotted in Figure 27. It can be seen from Figure 27 that although the intrinsic energy dissipation of the spin-wave-bus interconnects is lower than that of CMOS interconnects, the energy needed to excite spin waves can reduce the overall energy efficiency of spin-wave-bus interconnects. Plasmonic interconnects are more energy efficient up to a certain critical length that is determined by the propagation length of the plasmon through the plasmonic interconnect. The implementation of plasmonic interconnects at the local level requires plasmonic switches to avoid the energy and circuit-area overheads associated with signal conversion between electrical and plasmonic domains [179].

Performance factor (PF), energy factor (EF), and energy-delay-product factor (EDPF) for all novel interconnects are tabulated in Table 7 at an interconnect of length 10 gate pitches. Performance (Energy) Factor is defined as the ratio of the CMOS interconnect delay (energy) and the novel interconnect delay (energy) at the

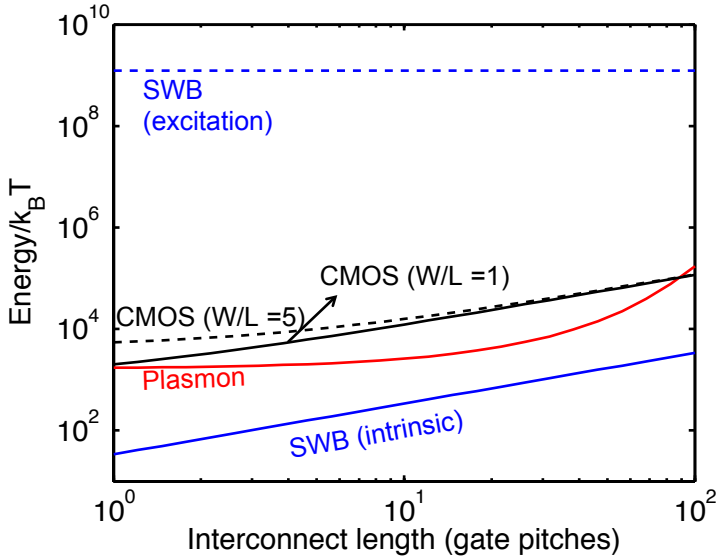

Figure 27: Energy dissipation versus interconnect length for wave-based interconnects. The propagation length of plasmons is assumed to be 3 μm. Two driver sizes for CMOS interconnects are considered: (i) W/L = 1(minimum-sized driver) and (ii) W/L = 5 (5× the minimum-sized driver).

same interconnect length. The energy-delay-product factor for a novel interconnect is defined as the product of its performance and energy factors at the same interconnect length. The performance factor for most interconnects (except plasmonic interconnects) is lower than unity. The energy factors of spin-diffusion and spin-wave bus interconnects is lower than unity. The results provided in Table 7 represent optimistic values as the device non-idealities in the new logic are not taken into account. The area-scaling factor to obtain the results in Table 7 is assumed to be unity. These numbers are expected to improve if the novel logic is scaled in area with respect to the CMOS logic.

2.4 System-Level Communication Metrics

Several communication metrics are used to benchmark the performance of interconnects. These metrics include delay, bandwidth, bandwidth-density per unit delay, power, and energy-per-bit. However, conventional interconnect metrics may not be

Table 7: Performance, energy, and energy-delay-product factors of various novel interconnects. Values are quoted at an interconnect length of 10 gate pitches and for a CMOS driver channel width-to-length ratio W/L = 5.

Interconnect	**PF**	**EF**	**EDPF = EF × PF**
Spin diffusion	0.03	0.83	0.025
Spin ballistic	0.86	23.24	20
Spin drift	0.32	4.82	1.56
Thermal diffusion	0.0038	4.04	0.015
Spin-wave bus ($v_{SWB} = 10^5 m/s$)	0.11	1.2×10^{-5}	1.29×10^{-6}
Plasmonic	122.6	6.03	739.1

very useful to benchmark new logic against the CMOS logic as the new logic switches can have drastic differences from the CMOS switches in terms of their delay, footprint, energy, and communication medium. Meaningful interconnect metrics that take into account the differences in novel logic families must be identified and defined to provide a universal platform for comparing interconnect aspects of various switches.

In this research, we use the following set of communication metrics to benchmark the various novel technologies against the CMOS technology:

- Signal-drive distance
- Clock locality
- Number of 2-input NAND gates accessible in one-clock cycle
- Square-bandwidth per unit area

Signal-drive distance (SDD) is a more powerful, scalable metric to understand the increasing wire delays and was first discussed by Doug Matzke in 1997 [141]. SDD is defined as the interconnect length for which the delay through that interconnect segment matches the intrinsic gate delay. SDD determines the relative balance of the speeds of switch and the interconnect. As the interconnect delay increases, SDD decreases necessitating the insertion of buffers in the design for optimal signal delay.

Conversely, a larger SDD means that there is less disparity in the delays of devices and interconnects. Another metric called the clock locality (CL) is also used to identify the growing interconnect problems in gigascale integration. CL represents the distance beyond which there is a need to insert a register in the design to resynchronize the signal with the local clock [141]. Consequently, a smaller value of CL means that the wire delay is a significant percentage of the overall signal delay. Assessing the number of 2-input NAND gates accessed in one-clock cycle for different technologies takes into account the varying footprints or area scaling of switches in the given technology. Square-bandwidth per unit area is a measure of the number of token escapes per unit area. It is obtained by multiplying the number of communication channels in the X-direction with the number of communication channels in the Y-direction in a 2-D paradigm. However, square-bandwidth per area must be modified in order to take into account the fact that same gates in different logic may differ in size. In other words, difference in switch density must be incorporated in this metric. Hence, the metric "square bandwidth per switch". This metric largely depends on area-scaling factor and the actual switch delays in the new technology. Hence, its actual value cannot be calculated without specific details concerning gate size and delays in the new technology. Therefore, we restrict ourselves to the metric "square-bandwidth per unit area" in this research.

To determine the system-level communication metrics for various novel technology options, the maximum allowable clock frequency needs to be first determined. Assuming that the longest local interconnect in the circuit has a time delay, $t_{longest,INT}$, that is no greater than 25% of the clock period, the minimum allowable clock period, $t_{min,CLK}$, is obtained as

$$t_{longest,INT} = 0.25 t_{min,CLK}, \tag{40}$$

where the longest interconnect in gate pitches is equal to $2\sqrt{N}$ in a circuit block with N gates. In Figure 28, the maximum allowable clock frequency for each novel

technology is plotted as a function of the number of gates in the circuit that are considered to be at the local level. The plasmonic system has the largest value of the maximum allowable clock frequency, while the phonon-diffusion system has the lowest value of the maximum allowable clock frequency. For diffusion-based novel systems, the maximum allowable clock frequency degrades as $1/N$, where N is the number of gates in the logic block. For all other novel logic systems, the maximum allowable clock frequency degrades as $1/\sqrt{N}$. Hence, from the perspective of clock frequency and bandwidth requirements, it may be important to have a small circuit size for the novel logic. However, smaller circuit size for the novel logic would require additional circuitry (and hence circuit area) for signal conversion into electrical domain. In addition, a smaller circuit area for novel logic would also mean additional power-overhead associated with signal conversion. Both circuit-area and power overheads associated with a small circuit area may be prohibitive for the novel logic.

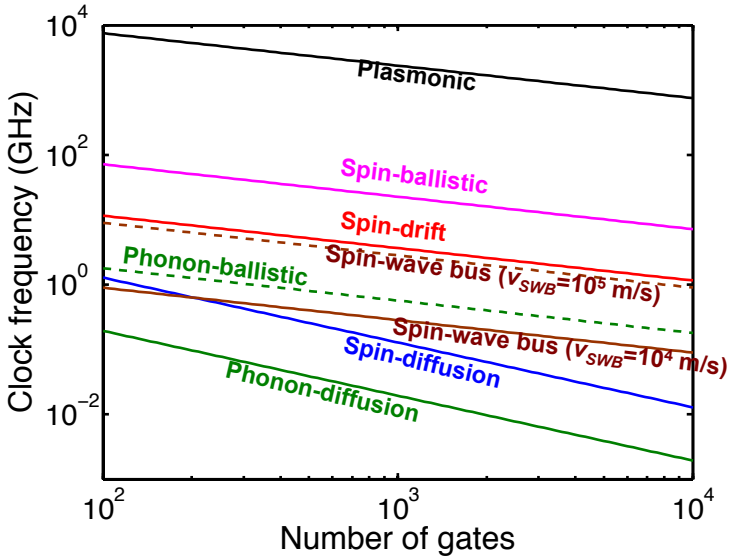

Figure 28: Clock frequency versus the number of gates in the logic block for various novel interconnects.

At the 2024 technology node, the on-chip local-clock frequency in the CMOS technology is $\approx$ 16.64 GHz as predicted by the ITRS [1]. The intrinsic delay of an

inverter driving only its parasitic load at the 2024 CMOS technology is roughly 0.27 ps, which is $\approx 225\times$ smaller than the on-chip clock period. Likewise, we can assume that the delay of an inverter in the new technology is $225\times$ smaller than the on-chip clock period. Choosing the number of gates in the novel logic to be 10^3, the system-level communication metrics for various novel interconnects are provided in Table 8. It is assumed that the area-scaling factor of each novel technology is equal to unity. The system-level communication metrics for CMOS system are also provided in Table 8. For CMOS interconnects, both the intrinsic delay of the interconnect and the impact of source resistance on the interconnect capacitance are taken into account. Amongst the various particle-based novel systems, spin-ballistic systems have the best square-bandwidth per unit area, and its value is even better than that in the case of CMOS interconnects. This conclusion is true if the upper bound on the circuit size of the spin-ballistic system is 1000 gates. The square-bandwidth per unit area scales as $1/N^2$ for diffusion-based systems, while it scales as $1/N$ for other novel systems. Hence, for a bigger circuit size the system-level communication metrics for novel technologies will degrade. Further, a better value of SDD in the case of novel systems when compared against CMOS systems only indicates that there is more disparity in the delays of interconnects and devices in the CMOS system than in the novel-logic system.

The actual values of the system-level communication metrics are highly dependent on the precise value of the clock frequency, the switch delay, and the switch footprint. However, if the increase in on-chip clock frequency is not augmented with a decrease in the interconnect delay, then the system-level metrics will be adversely affected and shall necessitate inserting more buffers and registers in the design.

Table 8: System-level communication metrics for novel interconnects for a circuit size of 1000 gates. Gate pitch is assumed to be 140 nm. No area scaling is considered for the novel technology. Hence, the footprint of a 2-input NAND gate in the novel technology is the same as that in the CMOS technology. CC stands for clock cycle. SQ-BW stands for square bandwidth.

Interconnect	**SDD**	**CL**	**(NAND gates)/CC**	**SQ-BW/area** $(GHz/nm)^2$
CMOS (electrical)	1	92	9.24×10^4	5.52×10^5
Spin diffusion	8.4	126.5	1.7×10^5	33
Spin ballistic	1.12	253	6.86×10^5	10^6
Spin drift	1.12	253	6.86×10^5	2.68×10^4
Phonon diffusion	8.4	126.5	1.7×10^5	0.753
Phonon ballistic	1.12	253	6.86×10^5	641
Spin-wave bus ($v_{SWB} = 10^5 m/s$)	1.12	253	6.86×10^5	1.56×10^4
Plasmonic	1.12	253	6.86×10^5	1.1×10^{10}

2.5 Conclusions

Interconnects impose major limitations in charge-based technology by consuming more than 50% of dynamic power in a microprocessor. In addition, interconnects also add delay to critical path and add noise and jitter to signals. Future device that are aimed towards using alternate state variable for information processing must be able to communicate their corresponding state variable in a fast and energy-efficient way at least locally. Otherwise, the energy and circuit-area overheads needed for signal conversion is going to be prohibitive for the new technology. A set of physical transport mechanisms are identified that may be employed to carry information encoded in various novel state variables. To provide a generic platform to compare emerging alternate technologies, the state variable is mapped against its corresponding transport mechanism. The particle-based transport mechanisms that are considered in this

research are diffusion (neutral and charged state variables), drift (charged state variables), and ballistic (neutral and charged state variables) transport. Amongst wave-based transport mechanisms, communication via spin waves and plasmonic waves has been considered in this research.

Physical models of performance and energy dissipation are developed for each transport mechanism as a function of the interconnect length in the system. An upper bound on the performance and energy dissipation of novel interconnects is obtained. It is found that most novel interconnects are relatively slow compared to their CMOS counterparts. Circuits utilizing alternate state variables can be competitive in terms of speed only if the interconnect lengths in them are shorter compared to those in CMOS circuits. Shorter lengths can be obtained (i) if the gate pitch of the new switches is scaled with respect to CMOS switches, and/or (ii) fewer switches are needed in the new logic to do the same task. Area scaling of new logic is defined as the ratio of the area of CMOS circuit and the new circuit (both of which implement the same function). It is found that new switches must be comparatively smaller in area. Area-scaling factors obtained for most novel interconnects are much larger than unity, which is quite challenging to achieve for new logic technologies.

System-level communication metrics such as signal-drive length, clock locality, number of 2-input NAND gates accessed in one-clock period, and square-bandwidth per switch are identified for the CMOS system and the new logic. For a circuit size of 1000 gates in the new logic, it is found that both signal-drive distance and the clock locality are superior in the case of novel logic systems as compared to those in the CMOS system. This is because there is a greater disparity in the device and interconnect delays in the CMOS system than in the novel logic systems for a clock period 4$\times$ the delay of the longest interconnect in a circuit consisting of 1000 gates for the novel logic. Improvements in signal-drive distance and clock locality for new interconnects come at the cost of lower square-bandwidth per unit area. The absolute

values of the metrics obtained in this thesis depend on the value of clock period chosen for the new logic. But it does not affect the conclusion that interconnect delays affect system-level metrics negatively. Moreover, if the increase in the chip clock frequency is not augmented with a decrease in the interconnect delay, then the system-level metrics will be adversely affected and shall necessitate inserting more buffers and registers in the design.

Novel logic with alternate state variables is likely to use a hybrid of new interconnects and electrical interconnects. While local interconnects shall be utilizing novel transport mechanisms for information transfer to avoid energy and circuit overhead associated with signal conversion, global interconnects are likely to be electrical.

CHAPTER III

MODELING TRANSPORT PARAMETERS IN SPIN INTERCONNECTS IN THE PRESENCE OF SIZE EFFECTS

Amongst the various novel state variables currently being researched for post-CMOS devices, electron spin is the most studied with proven advantages in terms of non-volatility, robustness, and storage density [9]. However, the potential advantages of electron-spin logic may be fully materialized only if electron spin is used both as an input and output of the new spin-based devices. If electron spin is used to solely control the flow of electric current in the new devices, then the same physical laws that are applicable to charge-based electronics will also be applicable to spin-based electronics. As described in Chapter II, electron spin may be communicated between spin devices in a spin fabric via an interconnect using diffusive, ballistic, quasi-ballistic, or drift transport mechanisms. The performance and the energy dissipation of spin interconnects is limited by material parameters of interconnects, such as the electron diffusivity, mobility, and the interconnect electrical resistance[1]. These material parameters degrade in the presence of size effects, particularly at narrow dimensions of the interconnect. As the dimensions of the on-chip interconnects shrink and become comparable to the electron mean free path, the scatterings of electrons at the surfaces and the grain boundaries are enhanced. These scatterings tend to lower the diffusivity and the mobility of electrons in materials, while increasing the interconnect resistivity. Therefore, size effects must be properly accounted for future technology

[1]For non-magnetic materials that will be used as interconnects in spin logic, the spin transport parameters are the same as the electron transport parameters.

generations to quantify the advantages, challenges, and limitations of the spin-based technology. While our primary intent is to use the results obtained in this chapter to quantify the limits of interconnects, these models can also be used by device engineers to analyze the performance of spin devices.

There are several non-magnetic materials that can serve as conduits of spin information in all-spin logic (ASL). Metallic conductors such as copper and aluminum have high conductivity and may help to overcome the issue of "conductivity mismatch"[2] between the transmitting magnet and the interconnect. The process technology for fabricating metallic conductors in ICs is quite mature and reliable.

The new carbon-based material graphene looks promising for interconnect and device applications in spin logic. This is because (i) graphene has a long electron mean free path (MFP), which directly translates into a high value for the electron diffusivity and mobility [70], [71]; (ii) using graphene as both the device and the interconnect may reduce the number of metal-to-graphene connections and may improve the performance of the circuit by eliminating some contact resistances; (iii) the spin-orbit coupling in graphene is quite weak because of the low atomic number of carbon $Z = 6$ [88] because of which the spin-relaxation length in graphene can be quite long. However, patterning graphene into narrow ribbons with smooth edges is a daunting challenge that needs to be addressed to materialize the potential of graphene for future technologies. The presence of edge roughness may degrade the mobility and the diffusion coefficient of electrons in graphene by an order of magnitude or more [180].

Semiconductor materials like silicon (Si) and gallium arsenide (GaAs) may also be used as both interconnects and devices in an all-spin logic. Silicon has been reported to have a long spin-relaxation length that can be tuned via the doping concentration.

[2]Conductivity mismatch refers to the difference in the conductivities of the spin-injecting magnet and the interconnect. The conductivity of semiconductors is much lower than that of the metallic ferromagnet, hence the efficiency of spin injection is drastically reduced in semiconductors.

GaAs is one of the most studied semiconductors for potential applications in spintronics. This is because it is easy to optically orient electrons in GaAs as it is a direct bandgap material [165], [55], [220].

In the next subsections, the physical models of electron mobility, diffusivity, and material resistivity for various materials are described.

3.1 Metallic conductors

Metallic conductors such as copper and aluminum may serve as spin interconnects in both conventional and non-local spin valves. The mobility of carriers in the interconnect is related to the effective resistivity of the interconnect material, ρ_{eff}, and the density of carriers in the interconnect, n_{3D}, as

$$\mu = \frac{1}{e n_{3D} \rho_{eff}}. \tag{41}$$

For materials with a parabolic band structure, n_{3D} is given as [6]

$$n_{3D} = 2\left(\frac{2\pi m^* k_B T}{h^2}\right)^{3/2} \mathcal{F}_{1/2}(\eta_F), \tag{42}$$

where h is the Planck's constant, m^* is the effective mass of electrons in the material, $k_B T$ is the thermal energy, $\mathcal{F}_{1/2}$ is the Fermi-Dirac integral with order $1/2$, η_F is the Fermi energy normalized to the thermal energy. The effective resistivity of metallic conductors in the presence of grain-boundary scattering is given by the Fuchs-Sondheimer model [204]. In the presence of side-wall scatterings, the Mayadas-Shatzkes model [142] is used. The combined effect of the grain-boundary and the surface scatterings on the effective resistivity, ρ_{eff}, of metallic conductors is given as [129]

$$\frac{\rho_{eff}}{\rho_0} = \frac{1}{3}\left[\frac{1}{3} - \frac{\alpha}{2} + \alpha^2 - \alpha^3 \ln\left(1 + \frac{1}{\alpha}\right)\right]^{-1} + 0.45(1-p)\frac{1+AR}{AR}\frac{\lambda}{W}, \tag{43a}$$

$$\alpha = \frac{\lambda}{d}\frac{R}{1-R}, \tag{43b}$$

where ρ_0 is the bulk conductor resistivity, λ is the bulk MFP of the electrons, W is the width of the conductor, d is average separation of the grain boundaries, R is the fraction of electrons scattered by the potential barrier at the grain boundary, p is the fraction of the electrons scattered specularly at the surface, and AR is the aspect ratio of the conductor. A list of the values of R for Cu extracted from experiments is given in Table 9. Table 10 shows the extracted values of R in aluminum. Only spin-valve experiments are considered. The value of sidewall specularity has been chosen to be either zero or 0.2 for extracting the values of R in Cu and Al. This is because the Cu/Ta interface is diffuse owing to a mismatch in the Fermi surfaces of Cu and Ta [186]. This leads to mostly diffuse sidewall scatterings in the case of copper. Hence, the value of p is relatively low for Cu interconnects. Further, the separation between the grain boundaries has been taken to be the minimum of the width or the thickness of the interconnect. For Al interconnects, similar assumptions are made.

Table 9: Extracted values of grain-boundary reflectivity, R, in copper.

Reference	**Value at $p = 0$**	**Value at $p = 0.2$**
F.J. Jedema et al, 2003 [93]	0.145	0.20
S. Garzon et al, 2005 [69]	0.65	0.66
Y. Ji et al, 2006 [95]	0.71	0.72
T. Kimura et al, 2008 [112]	0.48	0.51
X.J. Wang et al, 2009 [236]	0.19	0.23
H. zou et al, 2010 [251]	0.48	0.51

Table 10: Extracted values of grain-boundary reflectivity, R, in aluminum.

Aluminum		
Reference	**Value at $p = 0$**	**Value at $p = 0.2$**
F. J. Jedema et al, 2002 [92]	0.849	0.851
F. J. Jedema et al, 2003 [93]	0.011	0.084

Figure 29 shows the interconnect resistivity of Cu and Al versus the grain-boundary reflectivity at interconnect widths of 7.5 nm and 15 nm. Fully specular reflections at sidewalls are assumed. As the grain-boundary reflectivity, R, increases from 0.2 to 0.8, the effective resistivity of Cu increases by 8× and 10× for W = 15 nm and 7.5 nm, respectively. The corresponding increase in the effective resistivity of Al is 4.5× and 6× for 15 nm and 7.5 nm wide interconnects, respectively. Hence, size effects deteriorate the resistivity in Cu more than that in Al. In addition, the effective resistivity of Cu exceeds that of Al for all values of R ≥ 0.2 at W = 7.5 nm even with perfectly specular sidewall scatterings.

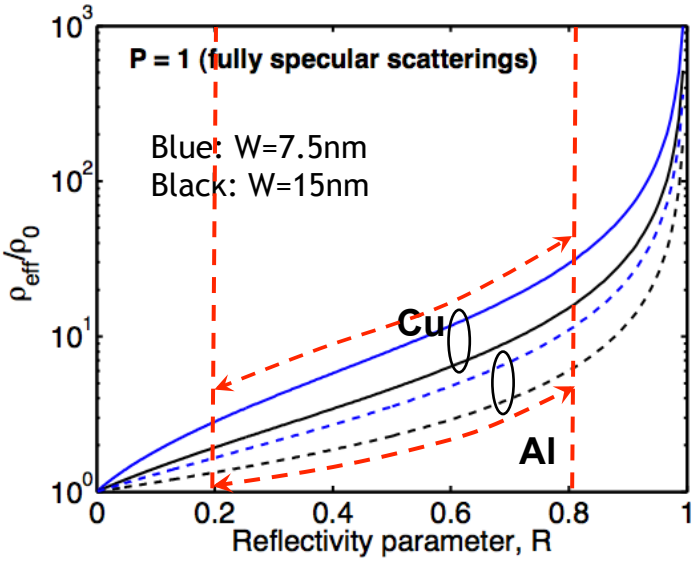

Figure 29: Effective resistivity of metallic conductors normalized to the bulk resistivity versus grain-boundary reflectivity. Increase in the resistivity of Cu is 10× and that of Al is 6× as R increases from 0.2 to 0.8 for W=7.5 nm (indicated by dashed red arrows).

The impact of sidewall specularity on the effective resistivity of metallic interconnects is examined in Figure 30. The impact of sidewall scatterings in changing the overall resistivity is only minimal compared to that of grain-boundary scatterings. Further, as the value of p has been realistically assumed to lie between zero and 0.2, it can be established that it is essentially the grain-boundary scatterings that

will determine the effective resistivity for Cu and Al. It can be seen from Figure 30 that as p changes from 0.2 to zero (diffusive sidewall scatterings), the increment in the effective resistivity of Cu is only 1.2× at $W = 7.5$ nm, even in the absence of grain-boundary scatterings.

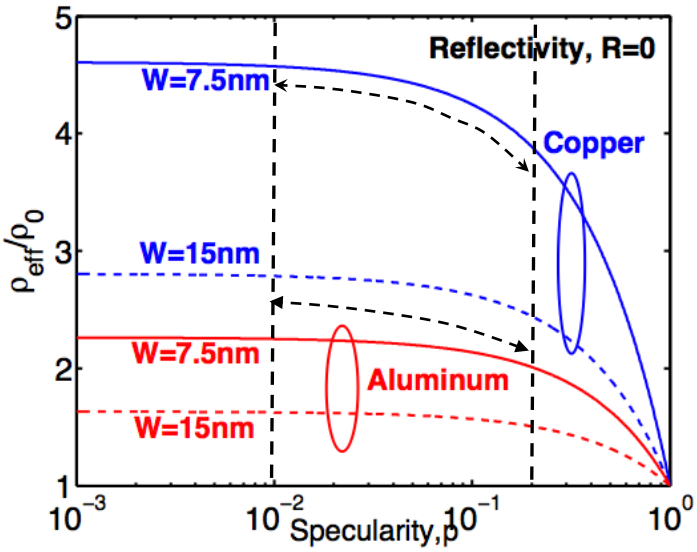

Figure 30: Effective resistivity of metallic conductors normalized to the bulk resistivity versus sidewall specularity. The impact of p in changing the effective resistivity of Cu and Al is only minimal even in the absence of grain-boundary scatterings (indicated by dashed black lines).

The mobility of carriers in Cu and Al as obtained in Eq. (41) is plotted as a function of the interconnect width at various values of the size-effect parameters in Figure 31. The values of the material parameters in the bulk to evaluate the transport parameters in Cu and Al are provided in Table 11. The best-case electron mobility in Cu is 44 cm^2/Vs, while that in Al is 13 cm^2/Vs. The best-case values do not scale with interconnect width. For a sidewall specularity $p = 0.2$ and an average grain-boundary reflectivity $R = 0.5$, the mobility of electrons in Cu degrades to 4 cm^2/Vs and that in Al degrades to 2.8 cm^2/s for an interconnect width of 7.5 nm. The degradation in the electron mobility of Cu interconnects is more than that of Al interconnects for similar size-effect parameters.

Table 11: Material parameter values for copper and aluminum interconnects.

Parameter	Copper	Aluminum
Bulk resistivity, ρ_0 ($\mu\Omega$-cm)	1.7	2.75
Mean-free-path, λ (μm)	0.04	0.014
Fermi energy, E_f (eV)	7	11.63
Density of electrons at Fermi level, n_{3D} (cm^{-3})	8.5×10^{22}	1.8×10^{23}
Fermi velocity, v_f (cm/s)	1.57×10^{8}	1.55×10^{8}

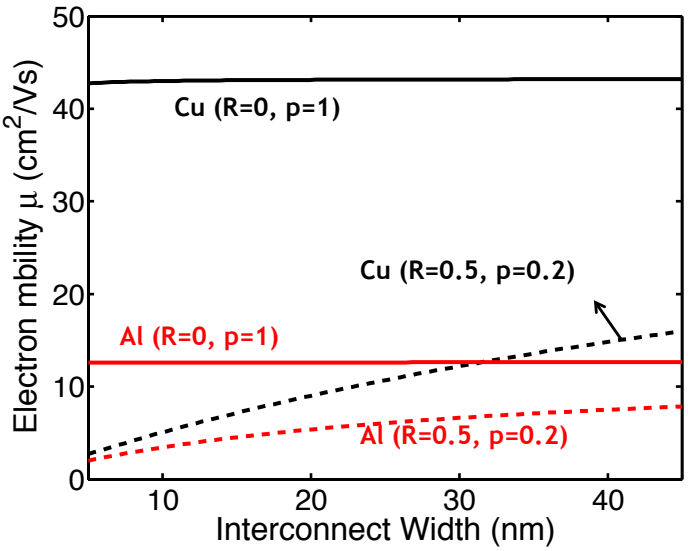

Figure 31: Mobility of electrons in Cu and Al interconnects as a function of the interconnect width for various size-effect parameters.

The relationship between the electron mobility, μ, and the diffusion coefficient, D, is governed by the Einstein's relation given as [243]

$$\frac{\mu}{qD} = \frac{\int_0^\infty DOS(E)\,(\partial f_{FD}/\partial E)\,dE}{\int_0^\infty DOS(E) f_{FD}(E) dE}, \tag{44a}$$

where $DOS(E)$ is the energy-dependent density of states of a three-dimensional conductor and is mathematically given as

$$DOS(E) = \frac{1}{2\pi^2}\left(\frac{2m^*}{\hbar^2}\right)^{3/2}\sqrt{E}, \tag{44b}$$

where m^* is the effective mass of electrons in the material, and $\hbar$ is the reduced

Planck's constant. Using (44a) and (44b), the diffusion coefficient of electrons for metals can be expressed in terms of their mobility as

$$D = \frac{2}{3\,(E_f/e)}\mu. \tag{44c}$$

Figure 32 shows the electron diffusion coefficient in Cu and Al versus the interconnect width in the presence of size effects. The best-case electron diffusion coefficient in the case of Cu is $\approx 200\ cm^2/s$, while in the case of Al it is $\approx 100\ cm^2/s$. For interconnect width $W = 7.5$ nm, the electron diffusion coefficient in Cu degrades to $18\ cm^2/s$ for $R = 0.5$ and $p = 0.2$. For the same parameters, the value of electron diffusion coefficient is $21\ cm^2/s$ in Al, which is slightly more than that in Cu. Hence, this result corroborates the fact that size effects degrade the transport parameters in Cu more than those in Al.

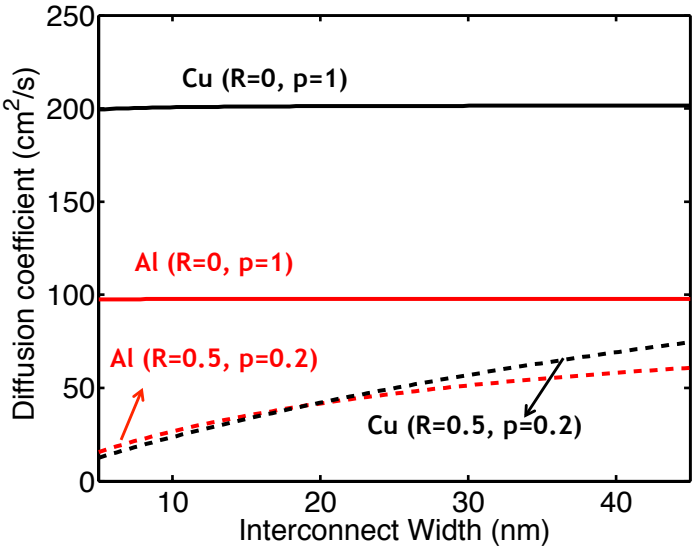

Figure 32: The diffusion coefficient of electrons in Cu and Al versus the interconnect width for various size-effect parameters. For interconnects narrower than 20 nm, electron diffusion coefficient in Al becomes better than that in Cu for $R = 0.5$ and $p = 0.2$.

The impact of sidewall scatterings on the electron diffusion coefficient in Cu and Al is examined in Figure 33. The electron diffusion coefficient in metals is not much

changed with sidewall specularity between zero and 0.2. A similar trend of electron mobility and effective material resistivity for metallic conductors on sidewall specularity was obtained earlier. The electron diffusion coefficient in Cu and Al is ≈ (45-50) cm^2/s at $R = 0$ and $W = 7.5$ nm. The value of electron diffusion coefficient degrades to ≈ 20 cm^2/s at $R = 0.5$ and $W = 7.5$ nm. In addition, the value of electron diffusion coefficient in Cu becomes slightly lower than that in Al for $R = 0.5$.

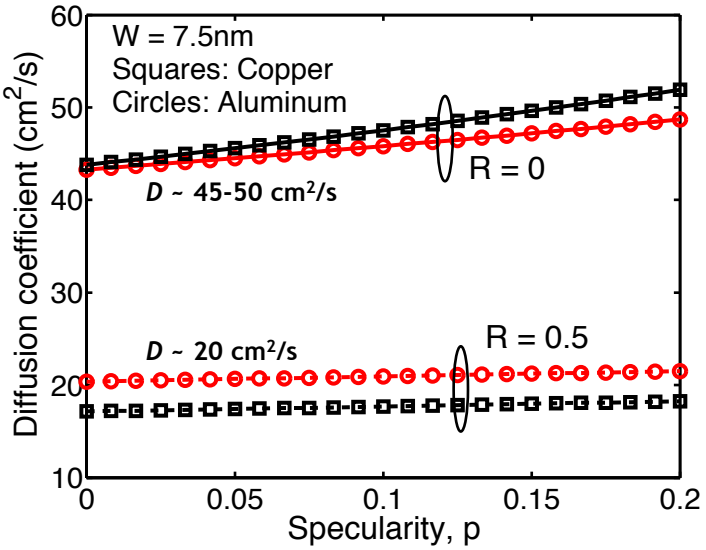

Figure 33: Diffusion coefficient in Cu and Al versus the sidewall specularity at an interconnect width of 7.5 nm for two values of grain-boundary reflectivity: (i) $R = 0$ and (ii) $R = 0.5$. Only a variation from zero to 0.2 for the sidewall specularity has been considered in accordance with the results from experiments.

3.2 Graphene

Graphene is a promising new material with potential applications for both spintronic devices and interconnects. Graphene offers a long electron MFP due to the limited phase space for scattering of electrons. Electron mobilities as large as 200,000 cm^2/Vs in 2D suspended graphene have been experimentally obtained [22]. However, many experiments also quote limited electron mobilities in graphene of the order of 1000 cm^2/Vs. The mobilities in these samples are limited by Coulomb scatterings due

to charged impurities in the substrate and/or due to resonant scatterers that induce mid-gap states in graphene [72]. Table 12 is a survey of the transport parameters obtained experimentally in graphene.

Table 12: A survey of experimental values of the electron mean free path and mobility in graphene.

Reference	**Substrate**	W (nm)	λ (nm)	μ (cm^2/Vs)
X. Wang et al, 2008 [235]	SiO_2	2.5	10	2000
W. Han et al, 2009 [79]	SiO_2	1900	67	–
X. Du et al, 2008 [53]	suspended	1400	1000	10^5 (T=100K)
K.I. Bolotin et al, 2008 [22]	suspended	3000	1200	2.3×10^5
J.L. Tedesco et al, 2009 [221]	SiC $(000\bar{1})$	10^4	–	1.5×10^5
T. Shimizu et al, 2011 [195]	SiO_2	100	(100-300)	–
A. Venugopal et al, 2011 [230]	SiO_2	180	–	2000
D.B. Farmer et al, 2011 [64]	SiC (0001)	1000	20	3000

There are several scattering mechanisms that limit the electron MFP in graphene. While the intrinsic sources of scatterings in graphene at finite temperature are due to acoustic and optical phonons, the extrinsic sources of scatterings are related to the substrate. The electron MFP in graphene due to acoustic phonons is given as [170]

$$\lambda^{AC} = 4\frac{\rho_m (\hbar v_f v_s)^2}{\sqrt{\pi N_s} D_{AC}^2 k_B T}, \tag{45}$$

where ρ_m is the mass density of graphene ($=7.6\times10^{-7}$ Kg/m^2), v_f is the Fermi velocity of electrons, v_s is the speed of acoustic phonons ($=20$ Km/s), N_s is the concentration of electron gas in graphene, and D_{AC} is the acoustic deformation potential. There is considerable uncertainty in the value of D_{AC} quoted in literature with typical values ranging from 6 eV to 30 eV [170]. Typically, D_{AC} is extracted from low-temperature

measurements assuming that the resistivity at low temperature is linearly proportional to temperature. The slope of the linear relationship between electrical resistivity and temperature is proportional to D_{AC}^2. However, this experimental procedure can only only provide an "effective" D_{AC} since the substrate effects on electrical measurements cannot be isolated even at low temperatures [125].

Scattering of electrons by non-polar optical phonons in graphene has an associated electron MFP which depends on the optical phonon energy and the electron-phonon coupling factor in addition to the electron energy and concentration. The electron MFP for scatterings by optical phonons is separated into two components representing the absorption or emission of optical phonons, which are mathematically given as

$$\lambda_{abs}^{OP} = \frac{\rho_m \hbar\omega_{OP} v_f^2}{\sqrt{\pi N_s} D_{OP}^2 N_{OP,abs} \left(1 + \frac{\omega_{OP}}{v_f\sqrt{\pi N_s}}\right)}, \tag{46}$$

$$\lambda_{emm}^{OP} = \frac{\rho_m \hbar\omega_{OP} v_f^2}{\sqrt{\pi N_s} D_{OP}^2 N_{OP,emm} \left(1 - \frac{\omega_{OP}}{v_f\sqrt{\pi N_s}}\right)}, \tag{47}$$

where $\hbar\omega_{OP}$ is the optical phonon energy (=160 meV), D_{OP} is the optical deformation potential, $N_{OP,abs}$ and $N_{OP,emm}$ are the phonon occupation numbers given by Bose-Einstein statistics for absorption and emission process, respectively. The emission process can only occur for electron energies greater than the energy of the optical phonon. The typical range of D_{OP} used in literature is (1-4)$\times 10^9$ eV/cm [170], [198], [63]. Away from the Dirac point where vacancies and inherent corrugations in graphene create localized states leading to a logarithmic correction in the density of states, it is phonons that set the upper limit on the electron MFP in graphene at any given temperature and finite carrier concentration.

The phonon-limited electron MFP in graphene is shown is Figure 34 as a function of carrier concentration for room temperature. The material parameters chosen for the simulation are provided in the legend. For low carrier concentration, the acoustic phonons limit the electron MFP in graphene. Once the optical-phonon emission process is activated for $N_s > 3 \times 10^{12}$ cm^{-2}, the net intrinsic MFP in graphene is

limited by optical phonon scatterings. At $N_s = 5 \times 10^{11}$ cm^{-2}, the MFP is 1.6 μm at R.T. for the material parameters chosen. If D_{AC} is chosen to be 10.5 meV, the electron MFP for the same carrier concentration will turn out to be 1.2 μm, which matches perfectly with the experimental result obtained by Bolotin & coworkers for intrinsic MFP in graphene [22].

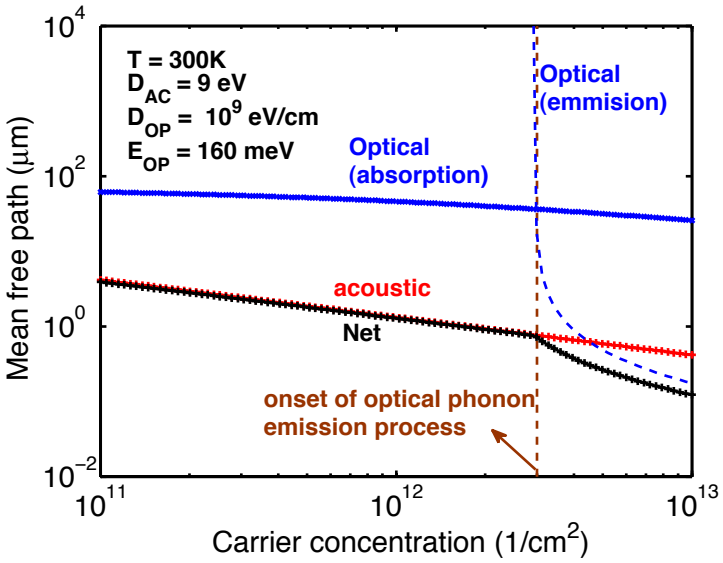

Figure 34: Electron mean free path limited only by intrinsic scattering sources in graphene versus carrier concentration at R.T.

The presence of charged impurities in the vicinity of the 2DEG in graphene sheet leads to a shift in the $\sigma - V_g$ characteristics of graphene along the V_g axis. There is always an inhomogeneity in the distribution of charges in graphene; this lateral inhomogeneity leads to an inhomogeneous distribution of the electrical properties of graphene, such as the electron MFP and the electron mobility. A recent experiment conducted by Giannazzo and coworkers in 2011 [72] to locally probe the charged impurity distribution using AFM in a wide graphene flake deposited on various substrates conclusively shows that the average density of charged impurities in SiO_2 is more than that in the case of SiC and STO substrates. A survey of the average concentration of charged impurities experimentally measured for graphene on various substrates is

given in Table 13. The table also shows the root mean square (RMS) of the surface roughness of the substrate. The surface roughness of the substrate is responsible for the creation of the electron-hole puddles, and a reduction in the surface roughness of the substrate could potentially lead to a reduction in the spatial distribution of charged impurities.

Table 13: Concentration of charged impurities and the root mean square of the surface roughness in graphene on various substrates. Data collected from [72], [48].

Substrate	**CI concentration (cm^{-2})**	**RMS of surface roughness (nm)**
SiO_2	$(1.3\text{-}1.8)\times10^{11}$	0.16±0.05
SiC	$(0.6\text{-}1)\times10^{11}$	0.17±0.05
$SrTiO_3$ (STO)	$(0.7\text{-}1.3)\times10^{11}$	0.2±0.05
h-BN	$< 7\times10^{10}$	≈ 0.03

The electron MFP in graphene limited due to charged-impurity (CI) scatterings is given as [208]

$$\lambda^{CI} = 16\frac{(\kappa_0\kappa\hbar v_f)^2}{Z^2q^4N_{CI}}\left(1+\frac{q^2}{\pi\hbar v_f\kappa_0\kappa}\right)^2\sqrt{\pi N_s}, \tag{48}$$

where κ is the average between the permittivity of the substrate and vacuum, Z is the net charge of the impurity, N_{CI} is the concentration of the impurity, and N_s is the two-dimensional carrier concentration in graphene. From the above equation, it is clear that the electron MFP due to CI scatterings increases if the permittivity of the substrate is higher. This is because a high-κ substrate can efficiently screen the Coulomb potential of the charged impurities. However, once the charged-impurity scattering is reduced, other sources of scattering particularly due to the surface polar phonons (SPP) in the substrate become more prominent. Due to the polar nature of the substrates used for graphene, a long-range polarization field that is associated with the lattice vibrations of the substrates gets electrostatically coupled to the electron

gas in graphene. Even though SPP scattering also exists in the case of metal oxide semiconductor field effect transistors (MOSFETs), it is relatively more important in the case of graphene because of the much small vertical dimension of the graphene sheet. The electron MFP in graphene limited due to SPP scatterings is given as [170]

$$\lambda_i^{SPP} = \sqrt{\frac{\beta}{E_i}} \frac{\hbar v_f 4\pi\kappa_0}{e^2} \frac{e v_f}{F_i^2} \frac{exp(k_0 z_0)}{N_{SPP,i}} \frac{\hbar\sqrt{\pi}}{e}, \tag{49}$$

where $\beta \approx 0.153\times10^{-4}$ eV, $z_0 = 0.35$ nm (separation between the graphene sheet and the substrate), $k_0 \approx \left[\left(2E_i\hbar^{-1}v_f^{-1}\right)^2 + \chi N_s\right]^{1/2}$, and $\chi \approx 10.5$. The index i denotes the polar phonon mode of the substrate, $N_{SPP,i}$ is the Bose-Einstein filling number of the i^{th} phonon mode, and F_i^2 is the Froehlich constant of the i^{th} mode. The Froehlich constant determines the magnitude of coupling between the electrons and the phonons. Substrates with a weak polarizability and higher phonon frequencies would lead to lesser electron-SPP scatterings. Further, the electrostatic coupling between the polar phonons of the substrate and the 2DEG in graphene becomes exponentially weaker with the spacing between the graphene sheet and the substrate. Hence, the electron MFP limited by SPP scatterings is ≈ 1.2 μm for a graphene sheet suspended 1 nm above h-BN versus an electron MFP of ≈ 0.9 μm for a graphene sheet directly on top of h-BN for an electron concentration $N_s = 5 \times 10^{11}$ cm^{-2}. Table 14 shows the parameters for SPP scattering for graphene on various substrates along with the electron MFP associated with SPP scatterings at R.T. for an electron concentration of 5×10^{11} cm^{-2}. The SPP-scattering-limited MFP is the best in the case of h-BN substrate (≈ 960 nm), while it is the lowest for HfO_2 substrate (≈ 30 nm).

The presence of resonant scatterers (RS) leads to a very weak D-peak in Raman measurements, where the intensity of the peak is directly related to the concentration of atomic-scale defects. In addition to adsorbates, inherent vacancies in graphene can also show D-peak in Raman measurements. Vacancies in graphene give rise to

Table 14: Parameters for surface-polar-phonon scattering in graphene for various substrates. Data collected from [170] and references therein. The electron MFPs are provided for R.T. at an electron concentration of 5×10^{11} cm^{-2}.

Property	**SiO_2**	**SiC**	**STO**	**h-BN**	**HfO_2**
κ_{sub}	3.9	9.7	330	5.09	22
E_1 (meV)	58.9	–	57	101.7	21.6
E_2 (meV)	156.4	116	92	195.7	54.2
F_1^2 (meV)	0.237	–	0.67	0.258	0.304
F_2^2 (meV)	1.612	0.734	1.082	0.52	0.293
λ_1^{SPP} (nm)	229	–	75.7	961	42.7
λ_2^{SPP} (nm)	1125	564	162.1	15000	156.6

localized states that hybridize with each other on an energy scale $E_{loc} \sim \frac{\hbar v_f}{R_1\sqrt{|\ln(R_0/R_1)|}}$, where R_0 is the radius of the RS $\approx 2a$, where a is the bond length of graphene, and R_1 is the average distance between the scatterers. For a concentration of resonant scatterers N_{RS}, R_1 can be approximately given as $1/\sqrt{N_{RS}}$. A Value of 10^{10} cm^{-2} has been experimentally measured for N_{RS} on a variety of substrates [72]. The electron MFP due to scatterings with RS is given as [208]

$$\lambda^{RS} = \frac{\sqrt{\pi N_s}}{\pi^2 N_{RS}} \left[\ln\left(\sqrt{\pi N_s} R_0\right)\right]^2. \tag{50}$$

The tradeoff between various scatterings limiting the electron MFP in graphene opens up an interesting problem of "substrate design", where an optimal substrate, in principle, will lead to minimal scatterings. The net electron MFP is given by the Mattheissen's rule, which can be stated as

$$\frac{1}{\lambda^{net}} = \frac{1}{\lambda^{AC}} + \frac{1}{\lambda^{OP}} + \frac{1}{\lambda^{CI}} + \Sigma_i \frac{1}{\lambda_i^{SPP}} + \frac{1}{\lambda^{RS}}. \tag{51}$$

In Figure 35, the electron MFP in graphene associated with various scattering mechanisms on various substrates is shown. The electron MFP is the best in the case

of h-BN substrate, and it is $\approx$ (2-3)$\times$ that of electrons in graphene on SiO_2. The electron MFP is a non-monotonic function of the carrier concentration. The MFP associated with scatterings due to SPP and CI increases with an increase in carrier concentration due to screening of the scattering potential by the charge carriers in the graphene sheet. The MFP associated with intrinsic acoustic and optical phonons scatterings decreases with an increase in carrier concentration. Hence, for electron concentration in excess of 3×10^{12} cm^{-2}, the electron MFP in graphene begins to degrade with an increase in carrier concentration.

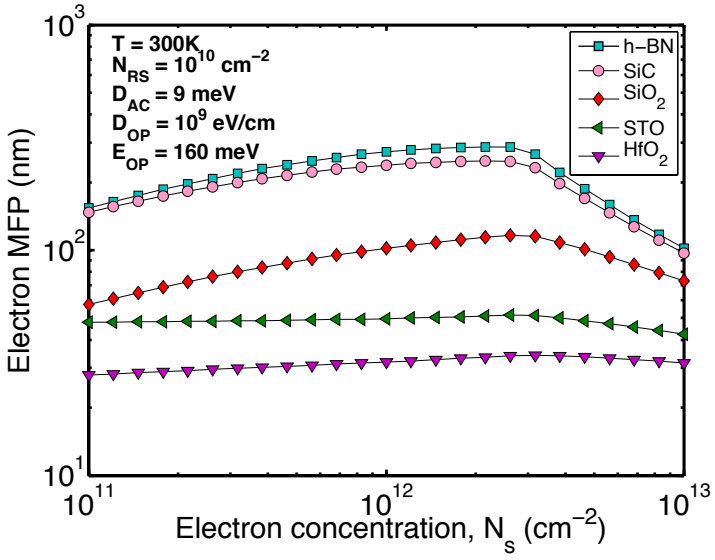

Figure 35: Electron MFP in graphene on various substrates at R.T. The parameter values are taken from Tables 13 and 14.

For bulk graphene, $D = 1/2\lambda^{net}v_f$. In Figure 36, the electron diffusion coefficient in graphene on SiO_2 is plotted as a function of the 2D carrier concentration. Also shown are the experimental data points from Jozsa et al. [99]. There is a reasonably good match between the experimental and theoretical results if the impurity concentration is selected as 4×10^{11} cm^{-2}.

The charge mobility in graphene versus electron concentration is shown in Figure 37. The electron mobility at R.T. for graphene on h-BN is 2.9×10^4 cm^2/Vs for an

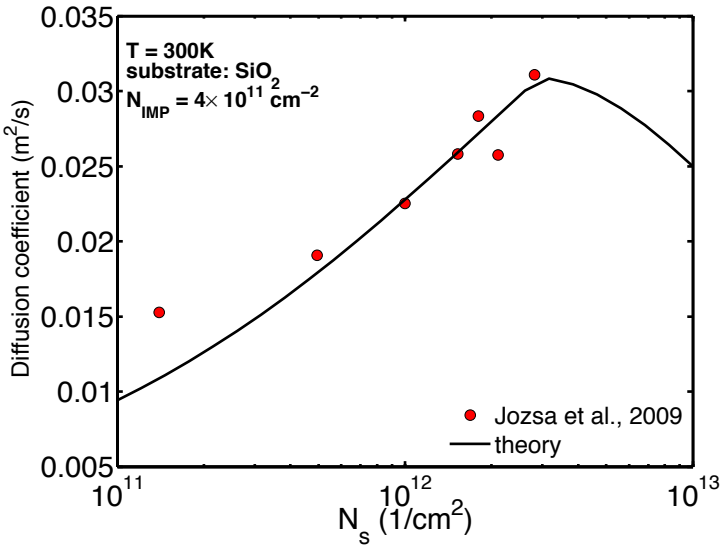

Figure 36: Diffusion coefficient in graphene at R.T. versus carrier concentration.

electron concentration of 5×10^{11} cm^{-2}, while the mobility degrades to 10^4 cm^2/Vs for graphene deposited on SiO_2 at the same carrier concentration. There is a good match between the experimental and theoretical values of electron mobility in graphene. Unlike electron MFP, which is a non-monotonic function of electron concentration, electron mobility in graphene decreases with an increase in carrier concentration.

For use as interconnects and devices in future technologies, graphene needs to be patterned into narrow ribbons. Semiclassical modeling has been applied in GNRs using tight binding (TB) calculations with ideal edges. From band-structure calculations, it can be shown that armchair graphene nanoribbons (GNRs) with ideal edges are semiconducting when the number of dimer lines is $(3M)$ or $(3M+1)$ (M is an integer), and semi-metallic when the number of dimer lines is $(3M-1)$; zigzag GNRs are all semi-metallic. Patterning graphene into narrow ribbons renders its edges rough. The presence of edge disorder can significantly modify the band-structure of graphene [176]. Due to roughness at the edges, the width of the GNR cannot be defined with atomic precision. Experiments show that all narrow GNRs are semiconducting with a bandgap that is independent of the orientation of the GNR and varies inversely with

the width of the GNR. Due to enhanced scatterings at the edges, the electron MFP in GNRs is significantly lower than that in 2D graphene[1].

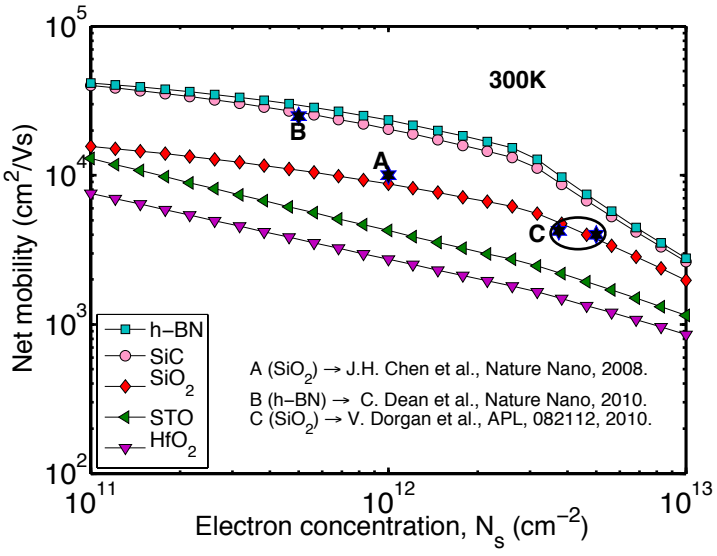

Figure 37: Electron mobility in graphene on various substrates. Simulation parameters are the same as in Figure 35.

Several approaches to model the electronic transport properties of GNRs have been discussed in literature [24], [25], [20], [63]. In the work by Bresciani & coworkers [24], a semi-empirical model of the dispersion relation in the GNR is suggested that replicates the density of states in the GNR calculated using TB with edge roughness. The semi-empirical E-k model resembles that of a 2D graphene sheet, but a cut-off energy for the density of states in the GNR is introduced as would be expected for semiconducting GNRs. In [63], the E-k dispersion relation of an armchair semiconducting GNR without edge roughness is used in conjunction with Boltzmann transport theory to model scattering rates due to various scattering sources present in the GNR. Betti & coworkers [20] perform atomistic simulations using 3D simulators like NanoTCAD ViDES based on NEGF formalism to obtain mobility in GNRs.

[1]Details on fabrication techniques to pattern GNRs with reduced edge roughness are given at the end of this section.

Here, we present a simple formalism to obtain the electron MFP in GNRs limited due to scatterings from the edges and the substrate. Since orientation effects are washed out in narrow GNRs, the E-k dispersion relationship of a semiconducting GNR that is obtained from TB calculation is used here. The E-k dispersion relation is given as

$$E = \hbar v_f \sqrt{k_{\parallel}^2 + k_{\perp}^2}, \tag{52}$$

where $k_{\parallel}$ is the wavevector along the length of the ribbon, and $k_{\perp}$ is the wavevector along the interconnect width, and it is quantized according to

$$k_{\perp} = \frac{\pi}{W}|m + \beta|, \tag{53}$$

where m is the sub-band index, W is the interconnect width, and $\beta = 1/3$ for semiconducting GNRs. The cut-off energy for the m^{th} sub-band is given as

$$E_{sub,m} = \frac{h v_f}{2W}|m + \beta|. \tag{54}$$

The low-field conductivity of GNRs is given using Landauer's formula according to

$$\sigma_{1D} = -\frac{2e^2}{h}\Sigma_m \int_{E_{sub,m}}^{\infty} dE \lambda_m(E) \frac{\partial f_{FD}(E)}{\partial E}, \tag{55}$$

where $f_{FD}(E)$ is the Fermi-Dirac statistics, $\lambda_m(E)$ is the electron MFP in the m^{th} sub-band in the GNR. The summation in Eq. (55) runs over all the conduction channels in the GNR. The number of conduction channels is a function of both the GNR width and the Fermi energy as shown in Figure 38. The number of conduction channels in the GNR increases with its width and the Fermi energy shift and with temperature. For GNRs with widths of 2.5 nm and 5 nm, the number of conduction channels at R.T. is less than unity for Fermi energies less than 0.3 eV and 0.15 eV, respectively.

The electron MFP of the m^{th} conduction channel in the GNR is obtained using the Mattheissen's rule for edge-scattering-limited MFP, $\lambda_m^{edge}(E)$, and the substrate-limited MFP, λ_{sub}, and it is given as

$$\frac{1}{\lambda_m(E)} = \frac{1}{\lambda_m^{edge}(E)} + \frac{1}{\lambda_{sub}}. \tag{56}$$

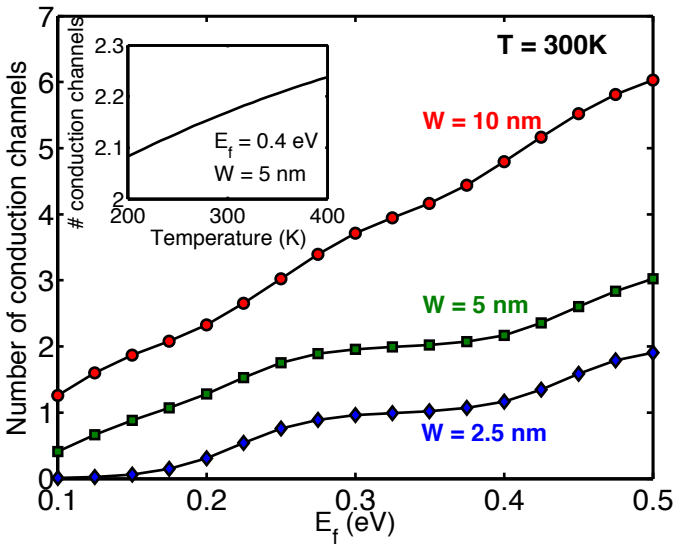

Figure 38: Number of conduction channels at R.T. versus the Fermi energy shift in the GNR for various GNR widths. The inset plot shows the impact of temperature on the number of conduction channels for a 5 nm wide ribbon at $E_f = 0.4$ eV.

As discussed in the previous section, the substrate-limited electron MFP in the GNR is $\leq$ 300 nm for typical Fermi-energy shift E_f = (0.2-0.4) eV in the GNR on top of h-BN. In the case of an "ideal" substrate that does not introduce any additional sources of electron scatterings in the GNR, the value of λ_{sub} will be limited by the intrinsic phonons in the graphene sheet, and in this case, $\lambda_{sub} \approx 1.2$ μm. The MFP associated with the diffusive scatterings at the edges is a function of the scattering probability at the edges and the average distance electrons move along the length of the ribbon before hitting one of the edges. This average length that electrons move in sub-band m without any scatterings is given by $v_{\parallel}/v_{\perp}$, where $v_{\parallel}$ and $v_{\perp}$ are the electron longitudinal and transverse velocities for the m^{th} sub-band. Knowing $v = -1/\hbar\,(\partial E/\partial k)$, the edge-scattering-limited MFP for the m^{th} mode can be given as

$$\lambda_m^{edge}(E) = \frac{1}{P_{GNR}}\frac{k_{\parallel}}{k_{\perp}}W = \frac{W}{P_{GNR}}\sqrt{\left(\frac{E}{E_{sub,m}}\right)^2 - 1}, \tag{57}$$

where P_{GNR} is the edge-scattering coefficient in the GNR. Values of P_{GNR} between 0.2

and unity are reported [17], [235]. An effective electron MFP, λ_{eff}, for the GNR is defined such that σ_{1D} from Eq. (55) can be expressed as

$$\sigma_{1D} = \frac{1}{R_Q}\lambda_{eff} N_{ch}, \tag{58}$$

where R_Q is the quantum resistance, and N_{ch} is the total number of conduction channels in the GNR. Hence, $\lambda_{eff} = \frac{\sigma_{1D} R_Q}{N_{ch}}$. The effective electron MFP is shown in Figure 39 as a function of the GNR width at various values of E_f and the substrate-limited electron MFP, λ_{sub}. For all GNR widths, the effective MFP increases with an increase in Fermi energy and the substrate-limited MFP. The electron MFP for a suspended wide graphene sheet measured by Bolotin & coworkers in 2008 is 1.2 μm for an electron concentration of 2×10^{11} cm^{-2} [22]. Even when the substrate-limited MFP is as high as 1.2 μm, there is more than 10× drop in the effective electron MFP of a 10 nm wide GNR with a 20% edge-scattering probability. For sub-10 nm GNR widths, the effective electron MFP will be limited to only few tens of nm, particularly for substrates like SiO_2 for which $\lambda_{sub} < 100$ nm. For GNR deposited on h-BN substrate with $\lambda_{sub} \approx 300$ nm, the effective electron MFP in a 10 nm wide GNR is 75 nm for $E_f = 0.2$ eV and 82 nm for $E_f = 0.4$ eV.

The electron diffusion coefficient in the GNR is related to its 1D conductivity, σ_{1D}, and the 1D density of carriers, n_{1D}, according to

$$D = \frac{\sigma_{1D}}{e^2 \frac{\partial n_{1D}}{\partial E_f}}, \tag{59}$$

where n_{1D} is obtained as the convolution of the density of states with the Fermi-Dirac distribution in the energy space, and it is mathematically given as

$$n_{1D} = \Sigma_m DOS(E) f_{FD}(E), \tag{60}$$

where $DOS(E)$ is the 1D density of states in graphene and $f_{FD}(E)$ is the Fermi-Dirac

distribution. The density of states is given as

$$\begin{aligned} DOS(E) &= \frac{2}{\pi}\frac{\partial k}{\partial E}, \\ &= \frac{4E}{h\nu_f\sqrt{E^2 - E_{sub,m}^2}}. \end{aligned} \tag{61}$$

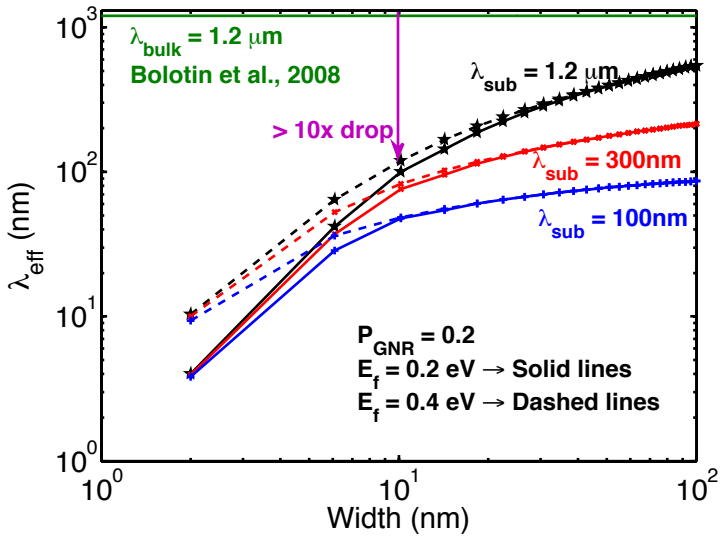

Figure 39: The effective electron MFP at R.T. versus GNR width for $P_{GNR} = 0.2$. For suspended graphene, an electron MFP of 1.2 μm as shown by the solid horizontal line is obtained experimentally by Bolotin et al. [22].

In Figure 40, the electron diffusion coefficient in GNRs is shown as a function of their width for various values of E_f and P_{GNR}. Like other electrical parameters, the electron diffusion coefficient in graphene is also adversely affected in the presence of size effects. As the interconnect width is decreased for $P_{GNR} = 0.2$, the diffusion coefficient degrades irrespective of the value of E_f. For $E_f = 0.2$ eV, there is a 3.1× degradation in the value of D at $W = 5$ nm when compared to its value for $W = 10$ nm. This degradation in D translates to an increase in the delay of the spin interconnect. The electron diffusion coefficient at narrow widths (< 10 nm) is slightly higher for $E_f = 0.4$ eV than for $E_f = 0.2$ eV.

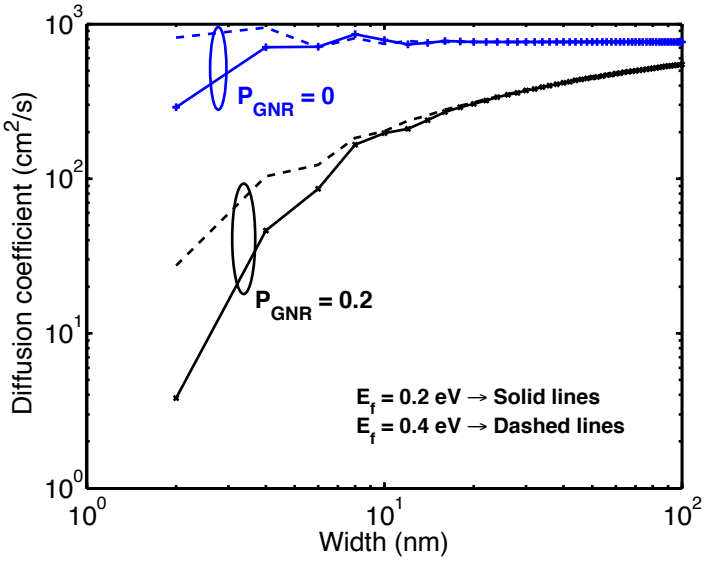

Figure 40: Electron diffusion coefficient in GNR as a function of its width for various values of E_f and P_{GNR}.

The electron mobility in GNRs is related to the 1D conductivity and the 1D carrier density according to

$$\mu = e\frac{\sigma_{1D}}{n_{1D}}, \tag{62}$$

where the 1D carrier density, n_{1D}, is given in Eq. (60). The electron mobility in GNRs is shown in Figure 41 as a function of the GNR width for various values of Fermi energy, the edge-scattering coefficient, and the substrate-limited MFP.

The electron mobility degrades with an increase in Fermi energy and the value of P_{GNR} at all interconnect widths. For an "ideal" substrate with λ_{sub} = 1.2 μm, the electron mobility of a 10 nm wide GNR can be as high as 2.8×10^4 cm^2/Vs at E_f = 0.2 eV and 1.5×10^4 cm^2/Vs at E_f = 0.4 eV. In the presence of edge roughness with P_{GNR} = 0.2, the electron mobility of a 10-nm wide GNR degrades to 2.3×10^3 cm^2/Vs for E_f = 0.2 eV, which is almost a 10× drop compared to its value at P_{GNR} = 0. For a 2.5 nm wide ribbon, the experimentally obtained value of mobility by X. Wang and coworkers [235] is ≈ 180 cm^2/Vs, and our simulations predict μ between (185-210) cm^2/Vs for E_f between (0.2 - 0.4) eV.

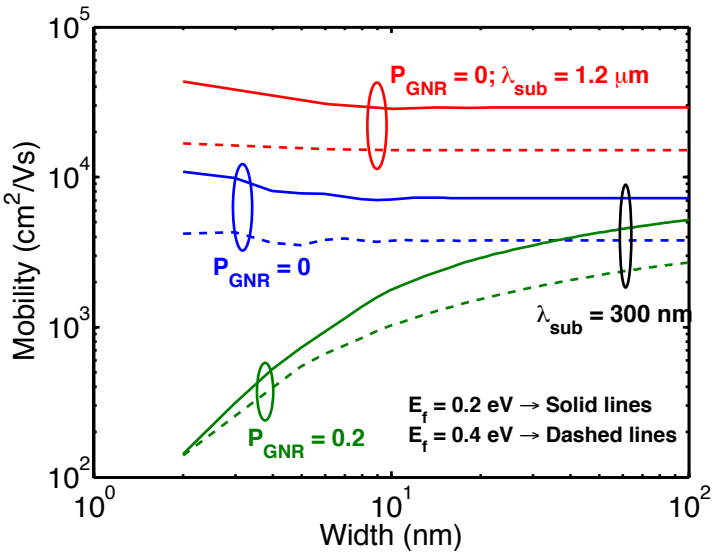

Figure 41: Electron mobility in GNRs as a function of their width.

The sheet resistance or the 2D resistivity of GNRs as a function of their width is plotted in Figure 42. The sheet resistance is given as the product $\sigma_{1D} \times W$. From Figure 42, it can be seen that the sheet resistance of the GNR improves with an increase in the Fermi energy resulting from an increase in the number of conduction channels in the GNR and an increase in the effective electron MFP in the GNR. The sheet resistance degrades drastically for sub-5 nm GNRs with a low E_f.

3.2.1 Multi-layer graphene nanoribbons

Graphene multilayers offer the advantage of additional conduction paths that can help to lower the resistance per unit length of the interconnect. Typically, in a multilayer GNR (ML-GNR), the contacts are fabricated on top as shown in Figure 43. The disadvantage of top contacts is that they are unable to provide perfect coupling to the layers beneath the top-most layer. In principle, the impact of non-zero resistivity of graphene along the c-axis on the overall resistance of the ML-GNR interconnect must be incorporated while assessing the advantage of ML-GNR interconnects over single-layer GNR (SL-GNR) and Cu/low-κ interconnects.

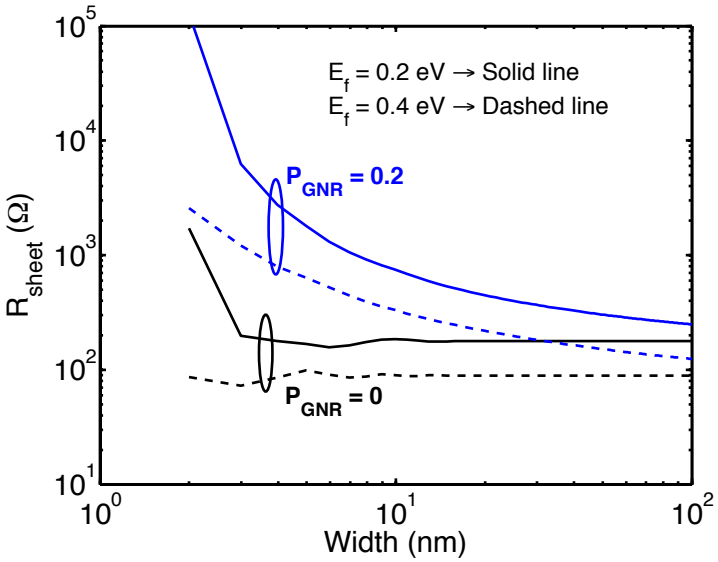

Figure 42: Sheet resistance of GNRs versus the width for various edge-scattering coefficients.

Following assumptions are made to proceed with the analysis of ML-GNR interconnects: (i) the ML-GNR system displays an E-k relationship similar to that of a monolayer GNR and (ii) the effective electron MFP in each layer depends only on the parameters of that layer. The first assumption is quite realistic especially in light of recent experimental findings in [65] and [229], where it was shown that the Raman spectra of few layer graphene (FLG) system grown epitaxially on carbon-terminated

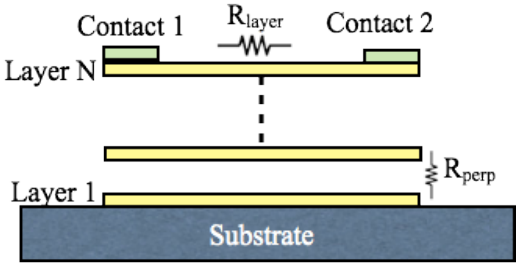

Figure 43: A 2D multi-layer graphene nanoribbon on top of a substrate. The multiple layers of the conductor are connected through a resistance R_{perp}. The in-plane resistance is denoted as R_{layer}.

face of SiC is identical to that of an exfoliated graphene monolayer. The same experimental observation was also reported for CVD grown FLG system in which there was no interlayer coupling between the parallel layers as confirmed by the electronic diffraction spectra [182]. The presence of stacking faults in the ML-GNR system leads to an apparent electronic decoupling of the layers. The second assumption used in the analysis follows from the first assumption if one treats all the layers independent of each other.

To evaluate the transport parameters in an ML-GNR, the effective resistance of the 2D structure is first obtained by incorporating the impact of interlayer resistance. The equivalent 2D distributed circuit diagram of ML-GNR is shown in Figure 44. The interconnect is assumed to have N layers, and each layer is partitioned into M segments along its length. The 2D resistance network may be split into $(N-1)$ unit cells, and the distributed components of in-plane and perpendicular resistances are denoted as R_b and R_a, respectively. Thus, R_b represents the resistance of a segment of a single-layer GNR with length dx, and R_a denotes the interlayer resistance between the layers having an overlap area of $dx \times W$. The top-most layer is treated separately when applying the boundary conditions. The resistances R_a and R_b are given as

$$R_a = \frac{\rho_m d_m}{W dx}, \tag{63}$$

$$R_b = \frac{R_Q dx}{\lambda_{eff}}, \tag{64}$$

where λ_{eff} is the effective MFP of electrons for a single layer, ρ_m is the c-axis resistivity, d_m is the spacing between the parallel layers. The c-axis resistivity for ML-GNRs will be treated as a parameter whose minimum value will be given by the c-axis resistivity of highly-oriented pyrolytic graphite (HOPG). The typical value of HOPG c-axis resistivity is (0.1-0.3) $\Omega.cm$ at R.T. [104], [225]. However, in the case of ML-GNR, the c-axis resistivity may be higher than that for HOPG because the layers in an ML-GNR network do not have the same crystallographic arrangement with respect

to each other as in the case of HOPG.

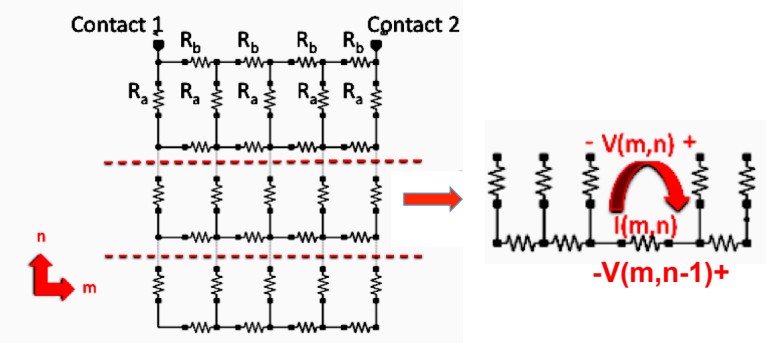

Figure 44: The distributed resistor network corresponding to the multi-layer GNR. The repeating unit to which KCL and KVL is applied is shown on the right.

The branch voltages and loop currents for the n^{th} layer are $V(m,n)$ and $I(m,n)$, respectively. The voltages vector, V_n, and the current vector, I_n, corresponding to the n^{th} layer are defined as

$$[V_n] = \begin{bmatrix} V(1,n) \\ V(2,n) \\ V(3,n) \\ . \\ . \\ . \\ V(M,n) \end{bmatrix} \&[I_n] = \begin{bmatrix} I(1,n) \\ I(2,n) \\ I(3,n) \\ . \\ . \\ . \\ I(M,n) \end{bmatrix}. \tag{65}$$

By applying KCL and KVL in an arbitrary layer n, the voltage vector $[V_n]$ and the current vector $[I_n]$ can be expressed in terms of $[V_{n-1}]$ and $[I_{n-1}]$ as

$$\begin{bmatrix} [V_n] \\ [I_n] \end{bmatrix} = \begin{bmatrix} H_v & R \\ G & H_i \end{bmatrix} \begin{bmatrix} [V_{n-1}] \\ [I_{n-1}] \end{bmatrix}, \tag{66}$$

where the transfer matrices H_v, H_i, G, and R are $M \times M$ matrices. Applying the

transfer matrix to $(N-1)$ layers,

$$\begin{bmatrix} [V_{N-1}] \\ [I_{N-1}] \end{bmatrix} = \begin{bmatrix} H_v & R \\ G & H_i \end{bmatrix}^{N-1} \begin{bmatrix} [V_0] \\ [I_0] \end{bmatrix}. \tag{67}$$

Hence, the overall transfer matrix is given as

$$\begin{bmatrix} H_{11} & H_{12} \\ H_{21} & H_{22} \end{bmatrix} = \begin{bmatrix} H_v & R \\ G & H_i \end{bmatrix}^{N-1} \tag{68}$$

By applying appropriate boundary conditions at layer-N, the effective electrical resistance of the ML-GNR between contact-1 and contact-2 in Figure 43 is given as

$$R_{eff} = \Sigma \left(H_{11} \times (H_{21} + H_{11}/R_a)^{-1} \right). \tag{69}$$

The net resistance by incorporating the impact of quantum resistances at the contacts is

$$R_{ML-GNR} = R_{eff} + \frac{R_Q}{N_{ch}}, \tag{70}$$

where N_{ch} is the number of conduction channels in the top-most layer of the ML-GNR stack. The impact of varying Fermi shift on the layer resistance may easily be incorporated in the model by multiplying the transfer matrix of each layer instead of assuming identical transfer matrices for all the layers.

The value of the number of partitions, M, along the interconnect length is chosen such that the maximum error in the effective resistance is less than 10-12% for any width, number of layers, and the interconnect length. The two extreme cases when the error is minimized are (i) $R_{layer} \gg R_{perp}$ and (ii) $R_{layer} \ll R_{perp}$. In case (i), the in-plane resistance is much more than the perpendicular resistance; hence, the layers can be assumed to be in parallel. In case (ii), the current flows mainly in the top-most layer of the multi-layer GNR. In both these cases, the number of partitions M does not affect the accuracy of the effective resistance. Figure 45 shows the error

plotted as a function of R_{layer}/R_{perp} for different values of M and $N > 4$. The error is calculated with respect to $M = 50$. The width, size effects, and the number of layers have a negligible impact on the peak value of the error. The error analysis shows that choosing $M = 10$ saves computational overhead without compromising the accuracy of analysis.

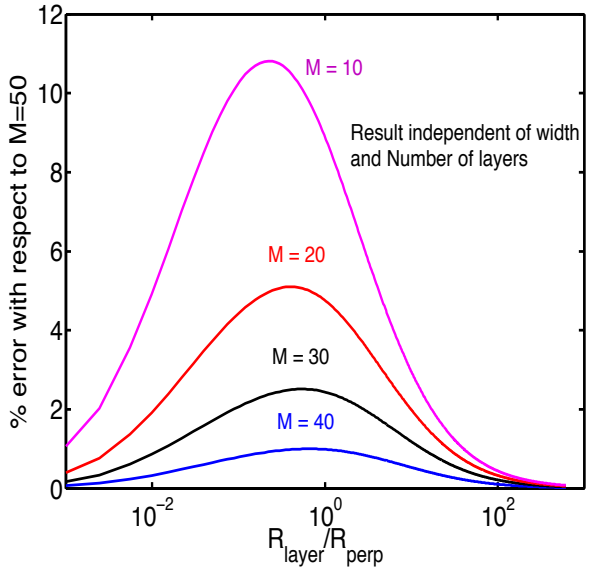

Figure 45: Plot of error versus R_{layer}/R_{perp} for different values of number of partitions, M, along the interconnect length. The error is calculated with respect to $M = 50$.

In the ideal case, all the layers within an N layer stack of ML-GNR will be available for conduction. Hence, the 1D conductivity of the ML-GNR in the ideal case should be $\sigma_{SL-GNR}N$, where σ_{SL-GNR} is the 1D conductivity of an SL-GNR. However, the presence of a non-zero inter-layer resistance reduces the number of layers available for conduction from the ideal case. The effective number of layers available for conduction is given by

$$N_{layer}^{effective} = \frac{\sigma_{ML-GNR}}{\sigma_{SL-GNR}}, \tag{71}$$

where σ_{ML-GNR} is computed with the physical number of layers, $N_{layer}^{physical}$. Figure 46 shows the effective number of layers versus the interconnect width for various values

of $N_{layer}^{physical}$ for interconnect of lengths of 1 μm and 10 μm.

For a high c-axis resistivity, $\rho_m \approx 100\rho_{m,HOPG}$, almost all the current conduction happens in the top-most layer for GNR with smooth edges. As the interconnect length is increased, the bottom layers start contributing to current conduction. For W >5 nm, only about four layers out of the 10 physical layers contribute to current conduction for L = 10 μm and P_{GNR} = 0. It is expected that with an increase in edge roughness of the GNR, more layers will contribute to current conduction. The effective number of layers that contribute to current conduction improves with a reduction in the c-axis resistivity of ML-GNR as shown in Figure 47. In general, the effective number of layers contributing to current conduction increase when the resistance of the top-layer of the GNR goes up either due to a reduction in its Fermi energy or an increase in its edge roughness. However, the fact that more number of layers contribute to current conduction may not necessarily translate to a reduction in the effective resistance of the ML-GNR stack. It can, however, be concluded with certainty that the effective resistance of the ML-GNR will be reduced upon a reduction of the c-axis resistivity.

The transport parameters such as the electron diffusion coefficient and the mobility in the ML-GNR will be governed by the characteristics of each layer. Since the Fermi energy is assumed to be identical for each layer and screening effects are ignored, the diffusion coefficient and mobility of electrons in the ML-GNR will be the same as that for SL-GNRs. These have been discussed in the previous section.

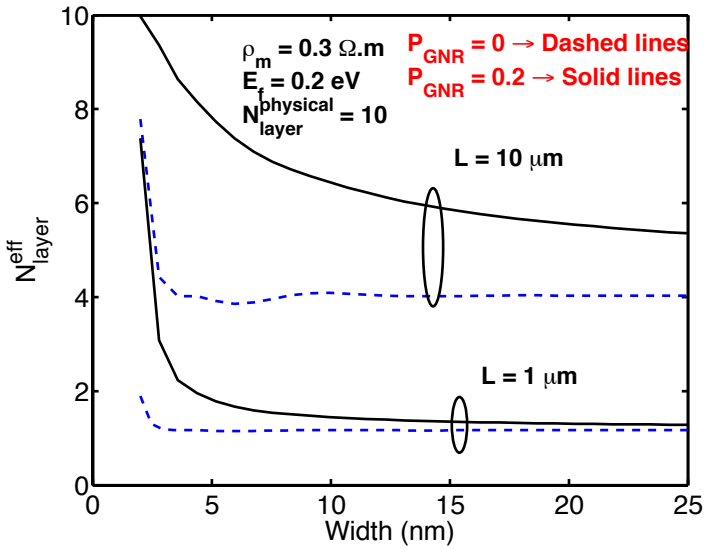

Figure 46: The effective number of layers contributing to current conduction as a function of interconnect width for various values of interconnect length and the edge-scattering coefficient. A value of c-axis resistivity that is 100× the resistivity of HOPG at R.T. is selected.

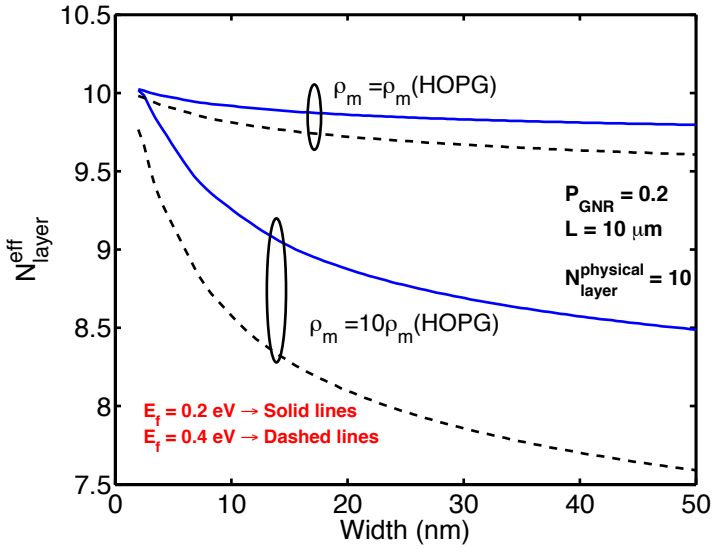

Figure 47: The effective number of layers contributing to current conduction in the ML-GNR stack versus the interconnect width for various values of the c-axis resistivity and the Fermi energy.

3.2.2 A survey of fabrication techniques for graphene nanoribbons

Both single- and multi-layer graphene nanoribbons may be suitable to serve as the channel material in high performance and low-power spin-valve circuits. However, the degradation in the spin transport parameters due to edge effects in GNRs must be addressed. Patterning narrow ribbons with width $\leq$ 10 nm needed for devices and interconnects introduces dangling bonds at the edges and degrades the otherwise attractive electron transport properties of graphene. Efforts to fabricate graphene nanoribbons with smooth edges are underway. Both lithographically and chemically-derived graphene nanoribbons have been experimentally demonstrated. Amongst the various methods, chemical vapor deposition has known advantages in terms of fabricating large quantities of graphene in a relatively short time. However, this method currently applies to wider graphene ribbons. For example, in 2008, thermal decomposition of ferrocene and tetrahydrofuran at 950°C produced $\approx$ 200 nm wide iron-filled carbon nanoribbons [136]. In the same year, researchers were also successful in fabricating a 40-layer GNR stack with widths between 20-300 nm using thermal decomposition of ferrocene/ethanol/thiophene solutions at 950°C [30]. However, the ribbons thus produced have many open edges. The current research efforts, therefore, must focus on fabricating smooth-edged graphene nanoribbons or otherwise passivating edges in these ribbons so that the superior electronic quality of graphene may be preserved down to sub-10 nm width for potential use in nanoelectronics. Table 15 provides a summary of experimental efforts to fabricate narrow graphene ribbons with reduced edge roughness.

Table 15: Experimental details on fabrication of graphene nanoribbons with reduced edge roughness.

Reference	Details
L. Xie et al, JACS 133, 2011 [241]	GNRs with widths between 10-30 nm were produced by sonochemical unzipping of multiwalled carbon nanotubes. Resistivity measurements showed that ribbons had lower edge roughness than those lithographically fabricated.
X. Wang and H. Dai, Nature Chem. 2, 2010 [234]	Conventional lithography in conjunction with gas-phase etching (high-T oxidation in presence of a slightly reducing environment) to produce smoother ribbons down to 5 nm. Lithography does produce appreciable edge roughness.
J. Cai et al, Nature Letters, 466, 2010 [29]	Bottom-up fabrication of atomically precise graphene nanoribbons. The topology, width, and edge periphery of GNR products are defined by the structure of the precursor monomers. The method is currently limited in approach to suitable substrates (eg. Au(111)).
M. Sprinkle et al, Nature Nanotechnology, vol. 5, 2010 [207]	Self-organized growth of ≈ 40 nm wide graphene ribbons on a templated SiC substrate using lithography.
K. Kim et al, ACS NANO, vol. 4, no. 3, 2010 [110]	Controlled thermally-induced unwrapping of multiwalled carbon nanotubes to produce 45nm wide graphene nanoribbons.

3.3 Semiconductors- Si and GaAs

Semiconducting materials like silicon and gallium arsenide may be well suited for interconnect applications in spintronics. Both devices and interconnects may be fabricated from the same material, thus, eliminating unwanted contact resistances. Further, the process technology for semiconductors is well established, which ensures no additional costs to change the process flow to fabricate spintronic devices and circuits. The transport parameters - electron diffusion coefficient, electron mobility, resistivity - may be easily tailored by controlling the dopant type and concentration in semiconductors. This provides a useful knob to achieve the desired properties in semiconductors for both device and interconnect applications in spin logic.

3.3.1 Silicon

Many semi-empirical models of electron mobility have been derived in literature for silicon because it is the single-most important semiconducting material for modern-day integrated circuits. These physical and semi-empirical models for the electron mobility of bulk silicon relate electron mobility to the carrier density and temperature. The Sah electron mobility model in silicon combines scattering rates due to acoustic and optical phonons via the Mattheissen's rule [162]. The ionized-impurity scattering is discussed in detail by Conwell-Weiskopf model [38] and the Brooks-Herring model [26]. Example of models that combine phonon and ionized-impurity scatterings in silicon are Dorkel-Letturcq model [51], Caughey-Thomas model [31], and Sharfetter-Gummel model [191].

In this research work, the electron mobility model developed by D.B.M. Klaassen [113] is used. The Klaassen mobility model provides a unified description of the majority-carrier and the minority-carrier mobilities by taking into account carrier-carrier scatterings, screening of impurities by charge carriers, and clustering of impurities. From the Klaassen mobility model, the electron mobility in Si due to phonon

scattering is given as

$$\mu_L = \mu_{max}\left(\frac{300}{T}\right)^{\theta}, \tag{72}$$

where μ_{max} is 1417 cm^2/Vs, and θ is determined in comparison with experimental data for bulk Si. The majority-impurity scattering mobility, μ_I, is given as

$$\begin{aligned}
\mu_I(N_I) &= \mu_N\left(\frac{N_{ref,1}}{N_I}\right)^{\alpha_1} + \mu_c, \\
\mu_N &= \frac{\mu_{max}^2}{\mu_{max}-\mu_{min}}\left(\frac{T}{300}\right)^{3\alpha_1-1.5}, \\
\mu_c &= \frac{\mu_{min}\mu_{max}}{\mu_{max}-\mu_{min}}\left(\frac{300}{T}\right)^{0.5},
\end{aligned} \tag{73}$$

where μ_{min}, $N_{ref,1}$, and α_1 are fitting parameters provided in Table 16 for arsenic- and phosphorus-doped n-type silicon and boron-doped p-type silicon. The net electron mobility is given by the Mattheissen's rule as

$$\frac{1}{\mu_{net}} = \frac{1}{\mu_L} + \frac{1}{\mu_I}. \tag{74}$$

Table 16: Fitting parameters for the semi-empirical model of electron mobility in bulk silicon. Taken from D.B.M. Klaassen, 1992 [113].

Parameter	Arsenic	Phosphorus	Boron
$\mu_{max}(cm^2/Vs)$	1417	1414	470.5
$\mu_{min}(cm^2/Vs)$	52.2	68.5	44.9
$N_{ref,1}(1/cm^3)$	9.68×10^{16}	9.2×10^{16}	2.23×10^{17}
α_1	0.68	0.711	0.719
θ	–	2.285	2.247

Figure 48 shows the electron mobility in silicon versus the phosphorus doping concentration at 300K. For comparison, the experimental data on the Hall mobility of silicon obtained by Graenacher and Czaja, 1967 [75] is also shown. There is an extremely good match between the theoretical model and the experimental results. The electron mobility in silicon degrades by an order of magnitude as the doping concentration increases from 10^{17} cm^{-3} to 10^{20} cm^{-3}.

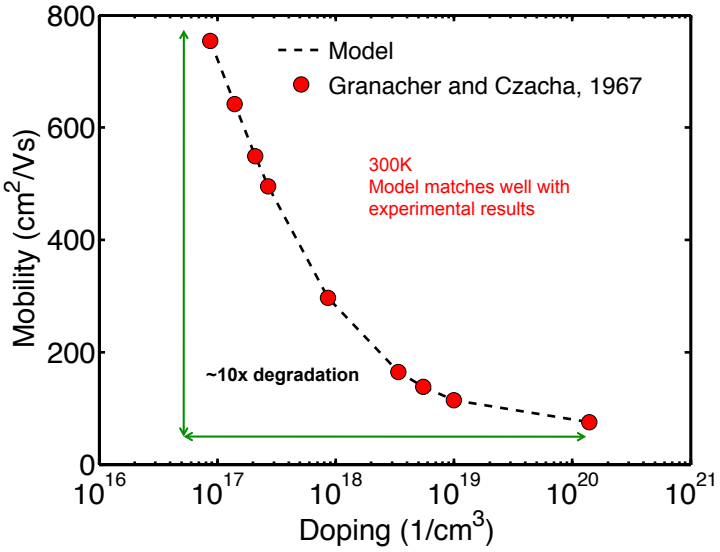

Figure 48: Electron mobility in silicon versus phosphors doping concentration. The lattice temperature is 300K. The experimental data on Hall mobility in Si:P from Granacher and Czaja, 1967 [75] is also shown.

The electron diffusion coefficient, D, in a given material is related to the electron mobility in the material according to Einstein's rule as in Eq. (44a). For non-degenerate semiconductors, the relationship between μ and D is

$$\frac{\mu}{eD} = \frac{1}{k_B T}. \tag{75}$$

For moderately-doped semiconductors, μ and D are related as

$$\frac{\mu}{eD} = \frac{1}{k_B T} \frac{\mathcal{F}_{-1/2}\left((E_f - E_c)/k_B T\right)}{\mathcal{F}_{1/2}\left((E_f - E_c)/k_B T\right)}, \tag{76}$$

where E_c is the bottom of the conduction-band edge, and $\mathcal{F}_n(\zeta)$ is the Fermi-Dirac integral of order n, which is mathematically given as

$$\mathcal{F}_n(\zeta) = \int_0^\infty x^n \left(e^{x-\zeta} + 1\right)^{-1} dx. \tag{77}$$

In the case of degenerately-doped semiconductors, the relationship between μ and D is given as

$$\frac{\mu}{eD} = \frac{3}{2(E_f - E_c)}. \tag{78}$$

To evaluate the electron diffusion coefficient, the position of the Fermi level in the semiconductor must be known. The position of the Fermi level shifts with the lattice temperature and the doping concentration in the semiconductor. The Fermi level, E_f, can be obtained by numerically solving the equation

$$n = N_c \frac{2}{\sqrt{\pi}} \int_0^\infty \sqrt{E} f_0(E - E_f) dE, \tag{79}$$

where n is the electron concentration in the semiconductor, N_c is the effective density of states of the conduction band in the semiconductor. The electron concentration in the semiconductor depends on the dopant concentration that is ionized, N_d^+, and is mathematically expressed as

$$n = -\frac{N_d^+}{2} + \sqrt{\left(\frac{N_d^+}{2}\right)^2 + n_i^2}, \tag{80a}$$

$$N_d^+ = N_d \zeta_d, \tag{80b}$$

where n_i is the intrinsic carrier concentration in the semiconductor, N_d is the dopant concentration, ζ_d is the degree of ionization of the dopant. When the dopant level is close to the Fermi level, the dopants states are occupied leading to only partial ionization. At very low dopant densities, most neighboring dopant atoms are situated far apart and their bound electrons do not interact with one another. This regime is characterized by a complete ionization of the dopant atoms. As the dopant density increases, most dopant states are filled even though all dopant atoms replace the host atom and are "electronically active". In this regime, as the dopant density increases, the degree of dopant ionization reduces. Beyond a critical doping density, the degree of ionization increases as the doping density increases. This is because the dopant clusters that form at high doping density connect with each other that helps electrons to move freely and increase the ionization degree of the dopant. The semi-empirical model of ζ_d as obtained by A. Schenk and coworkers in 2006 [192] is expressed as

$$\zeta_d = \frac{1}{1 + g_D \frac{n}{n_1}}, \tag{81}$$

where g_D is the effective degeneracy factor of the impurity in the semiconductor and is given as

$$g_D = \frac{b}{g + (1-b)\frac{N_d}{n_1}}, \tag{82}$$

$$n_1 = N_c exp(-\Delta E_d / k_B T), \tag{83}$$

$$b = \left[1 + \left(\frac{N_d}{N_{ref}}\right)^d\right]^{-1}, \tag{84}$$

where $\Delta E_d = (E_c - E_d)$ is the difference in the bottom of the conduction-band edge and the bottom of the dopant level in the semiconductor, and $g = 1/2$. The parameters N_{ref}, N_b, c, and d in the above set of equations are the fitting parameters depending on the type of the dopant species (see Table 17). The value of the dopant ionization energy, E_d, depends on the broadening of the dopant band in the semiconductor and is given as

$$E_d = \frac{E_d^0}{1 + (N_d/N_{ref})^c}, \tag{85}$$

where E_d^0 is the value of the dopant ionization energy in the absence of dopant energy-level broadening, N_{ref} and c are fitting parameters (see Table 17).

Table 17: Fitting parameters to calculate the degree of dopant ionization in silicon. Values taken from A. Schenk, 2006 [192].

Parameter	**Si: Phosphorus**	**Si: Arsenic**
N_{ref} (cm^{-3})	2.2×10^{18}	3×10^{18}
c	2	1.5
N_b (cm^{-3})	6×10^{18}	9×10^{18}
d	2.3	1.8
E_d^0 (meV)	45.5	54

The degree of ionization of phosphorus and arsenic in silicon at 300K as a function of the doping concentration is plotted in Figure 49. Previously, it was believed

that incomplete dopant ionization in the semiconductor is an issue only at low temperatures. However, the simulation results in Figure 49 show that even at 300K, the degree of ionization of phosphorus in silicon may only be 80% when the doping concentration is close to the metal-insulator transition point. The lowest value of the degree of dopant ionization in the case of arsenic-doped silicon is 75% and occurs at a doping value of $3{\times}10^{18}$ cm^{-3}. The landscape of ζ_d versus the doping concentration is divided into three distinct regions. Region I is characterized by a complete ionization and is limited to doping concentration less than 10^{16} cm^{-3}. In Region II, the degree of dopant ionization drops with an increase in doping and occurs for doping concentrations more than 10^{16} cm^{-3} but less than (2-3)$\times10^{18}$ cm^{-3} (the metal-insulator transition). Beyond a doping concentration of 3×10^{18} cm^{-3}, the degree of dopant ionization increases with doping concentration and becomes unity for doping concentrations higher than 10^{20} cm^{-3}.

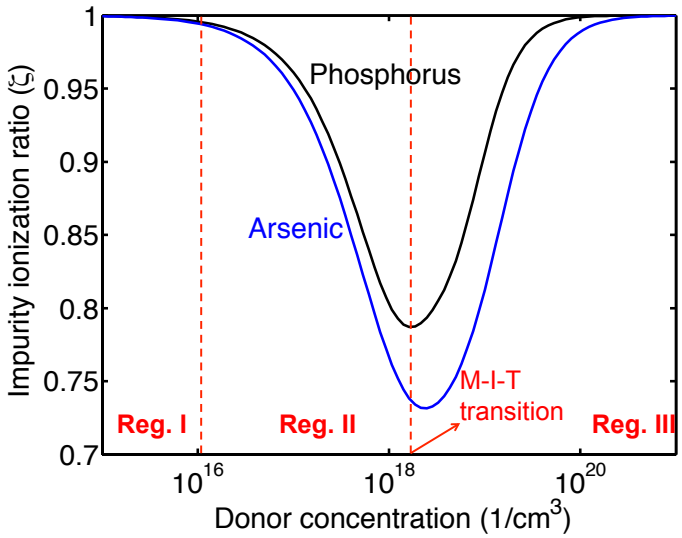

Figure 49: Degree of ionization of phosphorus and arsenic n-type dopant atoms in silicon host at 300K. Degree of ionization is minimum at $N_d = 1.8 \times 10^{18}$ cm^{-3}.

The position of the Fermi level relative to the conduction-band edge in silicon is shown in Figure 50 as a function of phosphorus doping at various temperatures. The

Fermi energy shifts towards the conduction-band edge as the doping increases, and beyond a doping level of 2×10^{19} cm^{-3} the Fermi level shifts into the conduction band. Having obtained the position of the Fermi level in silicon, Eq. (75) is used to plot the electron diffusion coefficient as a function of doping in Figure 51 for various lattice temperatures. It can be seen from Figure 51 that the diffusion coefficient drops by an order of magnitude as doping increases from 10^{14} cm^{-3} to 10^{19} cm^{-3}. The minimum of the diffusion coefficient is reached at the same doping level when the Fermi energy shifts into the conduction band. Beyond a doping level of 2×10^{19} cm^{-3}, the electron diffusion coefficient begins to increase with doping. The value of the electron diffusion coefficient for extremely low doping concentration in silicon is less than the best-case value of the electron diffusion coefficient obtained in the case of metals (Cu and Al) and GNRs.

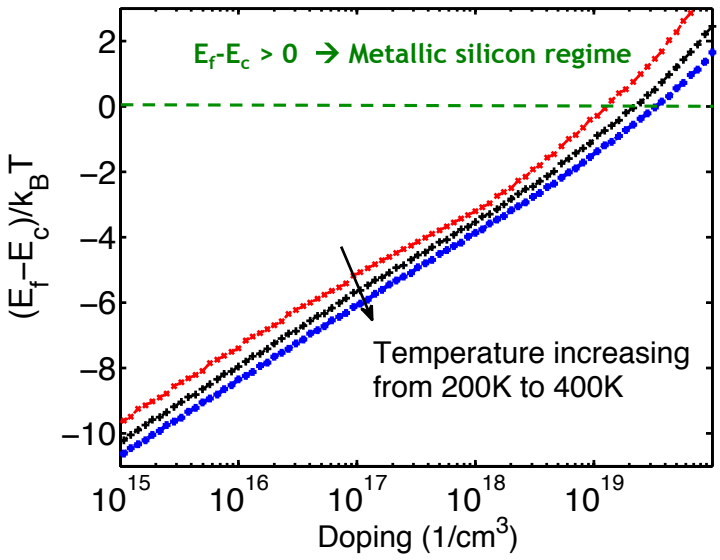

Figure 50: The position of the Fermi level relative to the conduction-band edge for various lattice temperatures in silicon. For $N_D > 2\times10^{19}$ cm^{-3}, the Fermi energy loves moves into the conduction band.

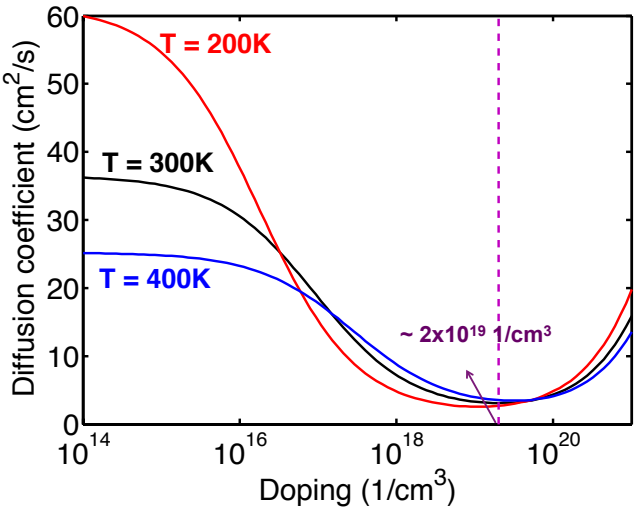

Figure 51: Electron diffusion coefficient in silicon versus doping concentration at various lattice temperatures.

For comparison, the theoretical model of electron diffusion coefficient in silicon is matched with experimental results as shown in Figure 52. There is a good match between the theoretical value of electron diffusion coefficient in silicon and the experimental values obtained by Sasaki and coworkers, 2010 [190] and Dash and coworkers, 2009 [40]. The experimental value of electron diffusion coefficient obtained by Li and coworkers, 2011 [128] is $\approx 2.5\times$ lower than the theoretical value. This is because the experiment by Li and coworkers was conducted at an extremely low temperature (10K) for which the Klaassen electron-mobility model in silicon may not be valid. Since the starting point for the calculation of electron diffusion coefficient is the mobility model, there could be a discrepancy between the theoretical and experimental values of D at low temperatures.

The resistivity of phosphorus-doped silicon as a function of doping concentration at 300K is shown in Figure 53. For comparison, experimental data on electrical resistivity of Si measured at 300K by Graenacher and Czaja [75] is also plotted in the figure. There is an excellent match between the theoretical and the experimental values. As the doping concentration increases from 10^{17} cm^{-3} to 10^{19} cm^{-3}, there is a

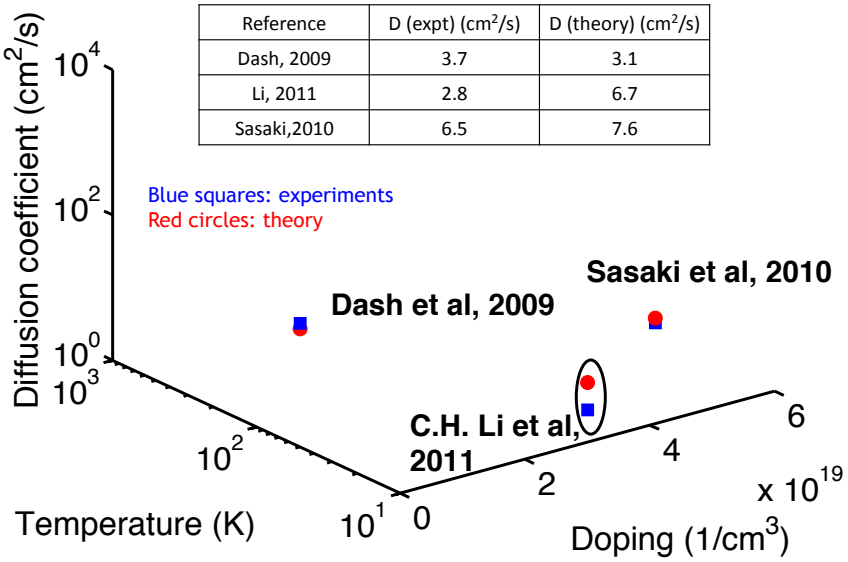

Figure 52: Experimentally measured electron diffusion coefficient in silicon for various doping concentrations and lattice temperatures.

10× reduction in the resistivity of silicon. This reduction in the material resistivity is especially important for achieving a high spin-injection efficiency with semiconducting interconnects in an all-spin logic. However, this improvement in conductivity of silicon is accompanied with a degradation in other spin-transport parameters (electron diffusion coefficient and mobility).

3.3.2 Gallium Arsenide

The low-field mobility in GaAs is obtained by considering the contributions to electron scattering from (i) acoustic phonons (ADP), (ii) ionized impurities (II), (iii) polar optical phonons (POP), and (iv) piezoelectric (PE) acoustic phonons. The Song-Kim (SK) mobility model [205] for GaAs is a physically-based mobility model that takes into account various electron scattering mechanisms and gives the electron mobility using Boltzmann electron statistics in a parabolic conduction band.

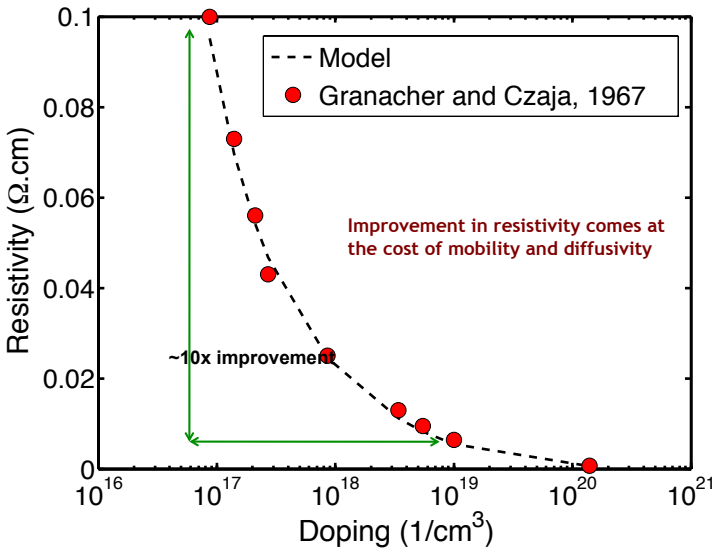

Figure 53: Resistivity of phosphorus-doped silicon versus doping concentration at 300K.

The net momentum-relaxation time, τ_p^{net}, obtained using the Mattheissen's rule is given as [205]

$$\frac{1}{\tau_p^{net}} = \frac{1}{\tau_p^{ADP}} + \frac{1}{\tau_p^{II}} + \frac{1}{\tau_p^{POP}} + \frac{1}{\tau_p^{PE}}. \tag{86}$$

The ADP-scattering-limited momentum-relaxation time in GaAs is given [205]

$$\tau_p^{ADP} = \frac{8\sqrt{\pi}}{3} \frac{\hbar R^{5/2}}{E_1^2 (k_B T)^{3/2}} \left(\frac{m_0}{m_c}\right)^{3/2} \frac{a_0^3 c_l}{R}, \tag{87}$$

where R is the Rydberg constant, m_c is the effective mass of the conduction electrons, a_0 is the Bohr radius, c_l is the average longitudinal elastic constant, and E_1 is the acoustic deformation potential.

The momentum-relaxation time due to electron and ionized-impurity scatterings is given using the Brooks-Herring approach as [205]

$$\tau_p^{II} = \frac{1}{3\pi^{3/2}} \frac{\epsilon_0^2 a_0^3}{2N_{min} + n} \frac{\hbar (k_B T)^{3/2}}{R^{5/2}} \left(\frac{m_c}{m_0}\right)^{1/2} \int_0^\infty \frac{x e^{-x}}{g(n, T, x)} dx, \tag{88}$$

where $x = E/k_B T$, N_{min} is the concentration of minority impurities (acceptors for

n-type GaAs), n is the electron concentration and is obtained by solving the equation

$$\frac{n(n+N_d)}{N_d - N_{min} - n} = \frac{N(T)}{2} e^{-E_i/k_B T}, \tag{89}$$

where N_d is the concentration of the donor species, $N(T) = \left(2m_c k_B T/(\pi\hbar^2)\right)^{3/2}/4$, and E_i is the ionization energy for the majority impurity. The function $g(n, T, x)$ in Eq. (88) is given as

$$\begin{aligned} g(n, T, x) &= \ln(1+b) - \frac{b}{1+b}, \\ b &= \frac{1}{2\pi} \frac{\epsilon_0}{a_0^3 n} \left(\frac{k_B T}{R}\right)^2 \left(\frac{m_c}{m_0}\right) x. \end{aligned} \tag{90}$$

The momentum-relaxation time due to electron and polar-optical phonon scatterings is given as [205]

$$\tau_p^{POP} = \frac{4}{3\sqrt{\pi}} \frac{\hbar}{\sqrt{R k_B T}} \left(\frac{\epsilon_0 \epsilon_\infty}{\epsilon_0 - \epsilon_\infty}\right) \left(\frac{m_0}{m_c}\right)^{1/2} \frac{e^{\theta_l/T} - 1}{\theta_l/T} G^{(1)} e^{-\zeta}, \tag{91}$$

where ϵ_0 and ϵ_∞ are the low- and high-frequency dielectric constants of GaAs, θ_l is the longitudinal optical phonon frequency (in the unit of temperature), ζ is the Fermi energy in the semiconductor normalized to the thermal energy, and the function $G^1(z)$ is given as

$$G^1(z) = \frac{9\pi}{32} \frac{e^{\zeta - 1/2z}}{z} (4z^2 + 9) \frac{K_1(1/2z) - 6zK_0(1/2z)}{2(z^2+2)K_1^2(1/2z) - zK_0(1/2z)K_1(1/2z) - 2z^2 K_0^2(1/2z)}, \tag{92}$$

where $z = \hbar\nu/k_B T$, K_0 and K_1 are the zeroth- and first-order modified Bessel functions of the second kind.

For the piezoelectric scattering, a spherical averaging over the piezoelectric and elastic constants over the zinc-blende structure gives the momentum-relaxation time as

$$\tau_p^{PE} = \frac{280\sqrt{\pi}}{3} \frac{\hbar}{\sqrt{R k_B T}} \left(\frac{m_0}{m_c}\right)^{1/2} \frac{R a_0/e^2}{h_{14}^2 \left(4/c_t + 3/c_l\right)}, \tag{93}$$

where h_{14} is the piezoelectric constant, c_l and c_t are the average longitudinal and transverse elastic constants, respectively. The values of the various material parameters in GaAs to obtain the net momentum-relaxation time are provided in Table 18.

Table 18: Material parameters in GaAs to evaluate the momentum-relaxation time. Values taken from P. Song, 2002 [205].

Parameter	Value
m_c/m_0	0.065
ϵ_0	12.515
ϵ_∞	10.673
θ_l	410K
c_l	1.4382×10^{12} dyn/cm^2
c_t	4.904×10^{11} dyn/cm^2
h_{14}	1.45×10^{7} V/cm
E_1	6.3 eV
N_c	7.5×10^{18} cm^{-3}

Several semi-empirical models for electron mobility in semiconductors have been developed to match the Hall mobility data obtained from experiments. One of the most frequently cited electron-mobility models is the Caughey-Thomas model [31]. Starting from the Caughey-Thomas mobility model with temperature-dependent parameters, Sotoodeh & coworkers [206] obtained a semi-empirical model to describe the electron mobility in GaAs. Their model provides a good fit with the available experimental data on Hall mobility in GaAs for a wide range of doping concentrations and temperatures. According to the Sotoodeh model, the low-field electron mobility in GaAs is given as

$$\mu(T) = \mu_{min} + \frac{\mu_{max}(300K)\,(300K/T)^{\theta_1} - \mu_{min}}{1 + \left(\frac{N}{N_{ref}(300K)(T/300K)^{\theta_2}}\right)^{\lambda}}, \tag{94}$$

where μ_{min}, μ_{max}, θ_1, θ_2, λ, and N_{ref} are the fitting parameters provided in Table 19. A relatively good fit is obtained for the carrier concentration range of 10^{13} cm^{-3} to 2×10^{19} cm^{-3} for n-type GaAs. A few limitations of this model are: (i) dopant compensation is ignored; (ii) mobility is considered independent of the dopant species; (iii) mobility is assumed independent of the growth method; (iv) effects of carrier-carrier and surface scatterings are not considered; (v) model is valid for relatively thick epitaxially-grown GaAs.

Table 19: Fitting parameters to obtain the mobility of electrons in bulk GaAs.

Parameter	**Value**
μ_{max}(300K) (cm^2/Vs)	9400
$\mu_{min} cm^2/Vs$	500
N_{ref}(300K) cm^{-3}	6.0×10^{16}
λ	0.394
θ_1	2.1
θ_2	3.0

Using the SK mobility model and the Sotoodeh mobility model for GaAs, the electron mobility is plotted in Figure 54 versus lattice temperature for a dopant concentration of 4.8×10^{13} cm^{-3} and an acceptor concentration of 2.13×10^{13} cm^{-3}. For comparison experimental data points from Woolfe & coworkers, 1970 [240] have also been shown in the figure. It can be seen from this figure that Sotoodeh mobility model cannot describe the experimental data for temperatures lower than 50K. The trend of mobility versus temperature for the experimental data matches with that of the SK model; however, the SK model predicts lower values of mobilities at a given temperature when compared to the experimental values for T $<$ 100K. In Figure 55, the experimental results on Hall mobility in n-type GaAs versus temperature is shown. The percentage difference between the experimental and theoretical values from Sotoodeh model is shown in the inset plot of Figure 55. It can be seen from this figure that Sotoodeh model is not able to describe the experimental results for temperatures lower than 100K or above 400K while keeping the error below 20%.

In Figure 56, the electron mobility in GaAs is plotted as a function of dopant concentration at 300K. It can be seen that the experimental data can be fit very well using the Sotoodeh model. As the doping concentration increases from 10^{13} cm^{-3} to 10^{18} cm^{-3}, the electron mobility drops from 8000 cm^2/Vs to 3000 cm^2/Vs at 300K. The electron mobility in GaAs is more than an order of magnitude higher than that in Si at the same temperature and for similar doping levels.

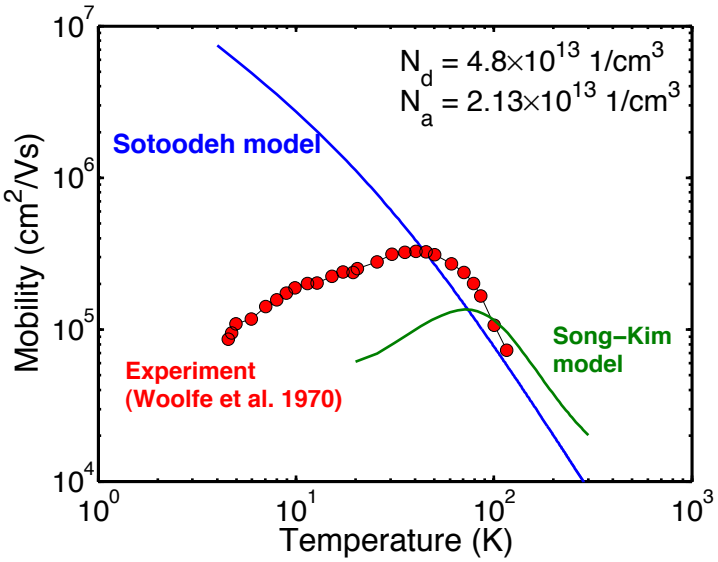

Figure 54: Electron mobility in GaAs versus lattice temperature using Song-Kim and Sotoodeh mobility models. Experimental data from Woolfe & coworkers, 1970 [240] is also shown for comparison.

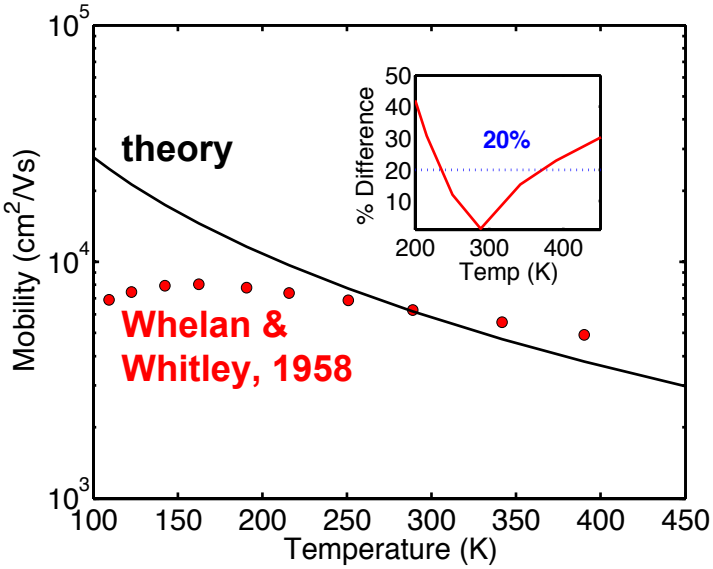

Figure 55: Electron mobility in GaAs versus lattice temperature using the Sotoodeh model. Experimental data is also shown for comparison. The inset plot shows the percentage difference between the theoretical values and experimental results (normalized to experimental values).

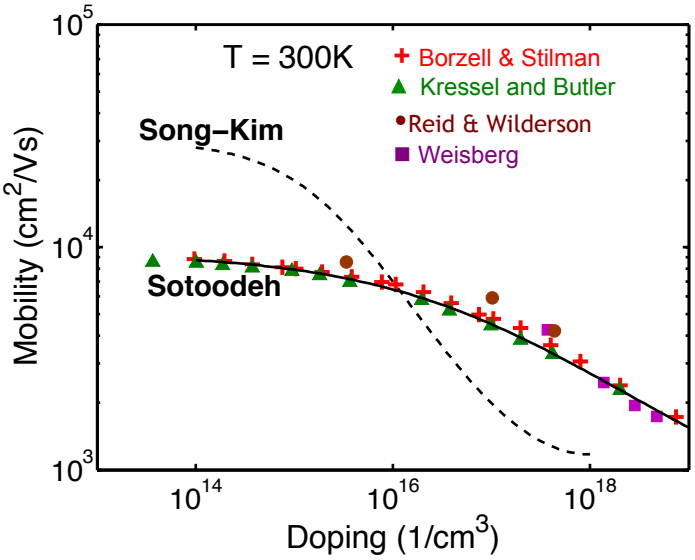

Figure 56: Mobility in GaAs versus doping concentration at 300K.

From the results shown in Figures 54-56, it can be concluded that Sotoodeh mobility model for majority carriers in n-type GaAs can explain the experimental results for temperatures between 100K and 400K and for doping concentrations between 10^{13} cm^{-3} and 10^{19} cm^{-3}. Hence, the Sotoodeh semi-empirical mobility model will be used to obtain the other spin transport parameters in GaAs.

The diffusion coefficient of electrons in GaAs is obtained using the Einstein's relation. However, to be able to use the Einstein's relation, the Fermi level in the semiconductor must first be determined. The Fermi level depends upon the free carrier concentration, which in turn depends on the ionized impurity concentration, N_d^+. Unlike in the case of Si, a piece-wise physically-based model for the degree of dopant ionization, ζ_d, in GaAs is used. For $N_d > N_{crit}$, ζ_d is equal to unity. For $N_d \leq N_{crit}$, ζ_d is given as

$$\zeta_d = \frac{N_d^+}{N_d} = \frac{-1 + \sqrt{1 + 4g_D\,(N_d/N_c)\,exp\,(\Delta E_d/k_B T)}}{2g_D\,(N_d/N_c)\,exp\,(\Delta E_d/k_B T)}, \tag{95}$$

where $g_D = 2$ is the degeneracy of the dopant atom, $\Delta E_d = (E_c - E_d)$ is equal to 6 meV for silicon dopant in GaAs.

Figure 57 shows the degree of ionization in GaAs as a function of doping concentration at lattice temperatures of 200K and 300K. For doping concentrations less than $N_{crit} = 2 \times 10^{16}$ cm^{-3} in GaAs [55], the degree of ionization drops with increasing doping concentration. At 300K, the drop in ζ_d is about 10%, while at 200K the drop is approximately 20% at $N_d = N_{crit}$.

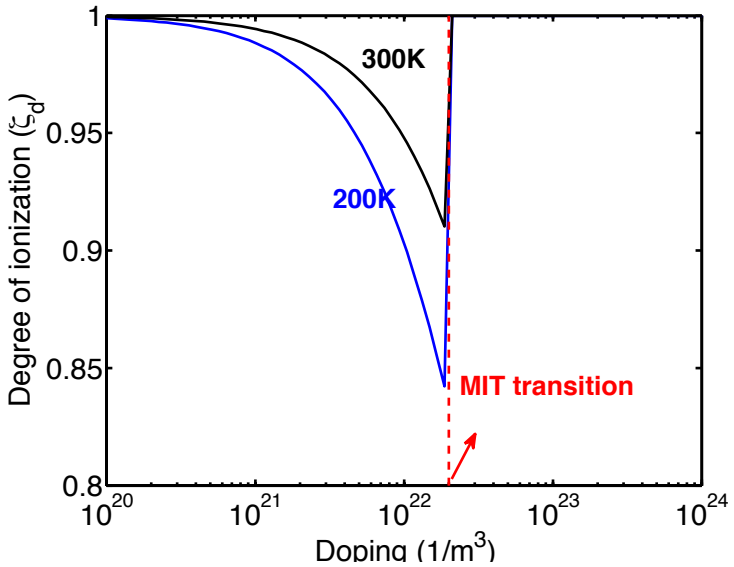

Figure 57: The degree of ionization versus doping concentration in GaAs at lattice temperatures of 200K and 300K.

The electron diffusion coefficient in GaAs is plotted in Figure 58 as a function of the doping concentration at various lattice temperatures. As the doping concentration increases, the electron diffusion coefficient in GaAs degrades for all temperatures considered in the analysis. At low-doping concentrations, the electron diffusion coefficient in GaAs is ≈ 200 cm^2/s at 300K. This value of electron diffusion coefficient is more than 5$\times$ larger than that in Si. The inset plot of Figure 58 shows the position of the Fermi level relative to the conduction-band edge in GaAs at various lattice temperatures. For doping concentrations greater than 3×10^{17} cm^{-3}, the Fermi level moves into the conduction band. Beyond this doping concentration, the electron diffusion coefficient in GaAs increases with increasing doping concentration.

The resistivity of n-type GaAs is shown in Figure 59 as a function of doping concentration at 300K. As the doping concentration increases from 10^{14} cm^{-3} to 10^{19} cm^{-3}, the resistivity of GaAs drops from 0.1 Ωm to 10^{-6} Ωm. For comparison, experimental data from Sze and Irwin, 1968 [219] is also shown in the figure. There is an extremely good match between the theoretical and experimental results. The inset plot of Figure 59 shows the temperature dependence of resistivity of GaAs with a silicon concentration of 10^{18} cm^{-3}. As the lattice temperature increases, the resistivity of GaAs increases. This is because of the degradation in electron mobility of GaAs as a function of temperature for the considered temperature range and doping concentration.

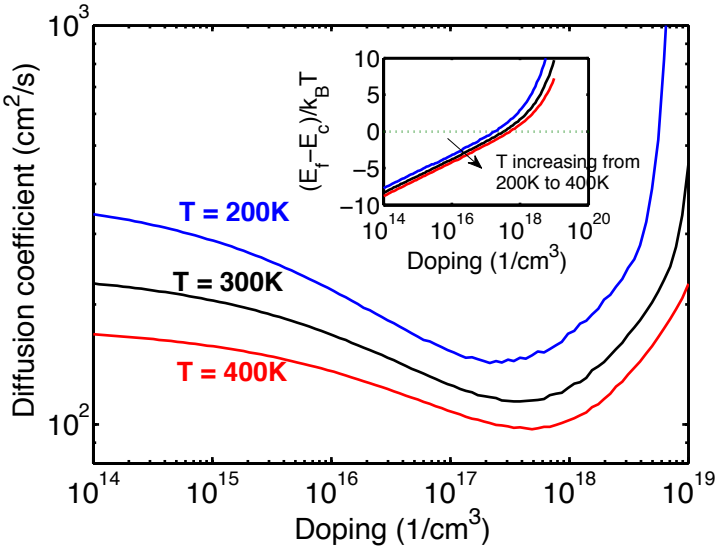

Figure 58: Electron diffusion coefficient in GaAs as a function of doping concentration at various lattice temperatures. The inset plot shows the position of the Fermi energy relative to the conduction band edge in GaAs.

3.3.3 Narrow width effects in GaAs

As the interconnect width scales to $\approx$ 7.5 nm for future technology generations, electrons within the semiconducting interconnect are confined within the potential barrier formed in the interconnect. The effects of quantum-mechanical confinement

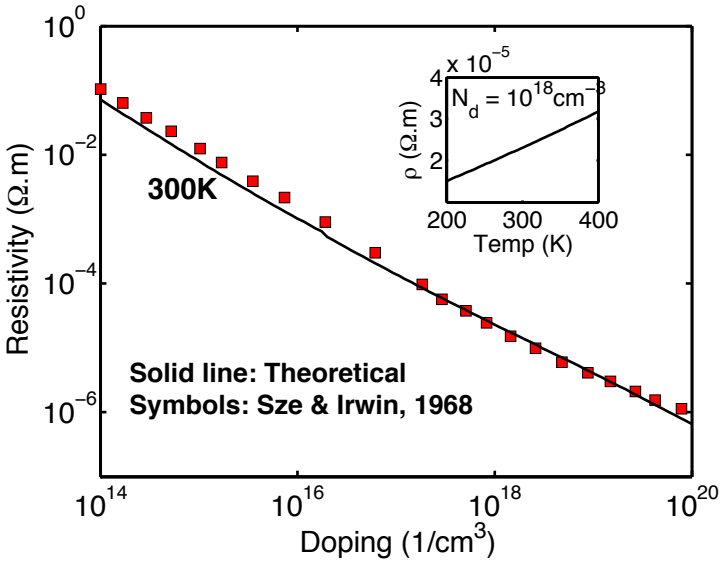

Figure 59: Resistivity versus doping in GaAs at various lattice temperatures.

of electrons in the interconnect must be considered if the width of the interconnect is smaller than the de-Broglie wavelength of the electrons. That is,

$$W \leq \lambda_{de-Broglie} = \frac{\hbar}{\sqrt{3 m_z k_B T}}, \tag{96}$$

where m_z is the effective mass of conduction-band electrons in silicon and is $\approx 0.916\times$ the free electron mass, which makes $\lambda_{de-Broglie}$ of electrons in silicon 6.3 nm. Hence, for an interconnect width of 7.5 nm quantum-confinement effects may not be important to consider for silicon-based interconnects. However, the $\lambda_{de-Broglie}$ of conduction electrons in GaAs is 24 nm. Hence, electron-confinement effects for a 7.5 nm wide quantum well must be properly accounted for to evaluate the transport parameters for GaAs-based interconnects.

To evaluate the scattering rate of electrons within the quantum well, it is assumed that the interconnect provides an infinite, square potential well to confine the electrons. This makes the quantized energy levels within the quantum well

$$E_n = \frac{(n\pi\hbar)^2}{2 m_z W^2}, \tag{97}$$

where m_z is the mass of the confined electrons. The wavefunction of electrons within the infinite, square potential well is given as

$$\psi(z) = \left(\frac{2}{W}\right)^{1/2} \sin\left(\frac{\pi z}{W}\right). \tag{98}$$

The assumption of the interconnect being an infinite quantum well may be justified if the penetration depth of the wavefunction within the barrier is much smaller than the well width. The penetration of the wavefunction within the barrier leads to a distortion of the wavefunctions in the quantum well, which results in corrections in the scattering matrix elements; these corrections are negligible if the band offset between the well and the interface is large enough. To evaluate the net momentum-relaxation time of electrons in the quantum well, only single-subband transport is considered. For a GaAs interconnect width of 7.5 nm, the difference in the minimum energy levels of the first and the second subbands in GaAs is greater than $10k_BT$ at room temperature. Hence, if the Fermi level is more than $3k_BT$ below the second band, the assumption of a single-subband transport is justified. The approach adopted to obtain the momentum-relaxation time in quantum wells is described in [74], [209], [175]. Following the work of Laikhtman and Kiehl, 1993 [119], the momentum scattering rate in a 2D quantum well for elastic scattering within the well may be given as

$$\frac{1}{\tau} = \frac{m_{DOS}}{\pi\hbar^3 k^2} \int_0^{2k} \frac{|M(q)|^2}{(1 + q_s/qH(q)\Pi(0,q))^2} \frac{q^2}{\sqrt{4k^2 - q^2}} dq, \tag{99}$$

where $|M(q)|^2$ is the scattering matrix element, q is the wave-vector transferred to the electron during the scattering event, m_{DOS} is the density-of-states mass of electrons and is given as $\sqrt{m_x m_y}$, q_s is the screening parameter, $H(q)$ is the screening matrix element that is a form factor depending on the wavefunction of the electron and electric-field distributions, and $\Pi(0,q)$ is a dimensionless polarization operator describing the response of the 2D gas on external perturbations. The mathematical

expressions for q_s, $H(q)$, $\Pi(0,q)$ are [119]

$$q_s = \frac{2m_{DOS}e^2}{\kappa_1\hbar^2}, \tag{100}$$

$$H(q) = \frac{2}{qW} + \frac{qW}{(qW)^2+4\pi^2} - \frac{32\pi^4}{(qW)^2\left[(qW)^2+4\pi^2\right]}\left(1-e^{-qW}\right), \tag{101}$$

$$\Pi(0,q) = \int_0^1 \frac{dx}{1+exp\left(\frac{E_q}{4k_BT}(1-x^2)-\frac{E_f-E_1}{k_BT}\right)}, \tag{102}$$

where e is the electron charge, W is the width of the quantum well, κ_1 is the dielectric constant in the quantum well, E_f is the Fermi energy of the electron gas, and E_1 is the first quantized energy level of electrons confined within the quantum well. In obtaining Eq. (102), it is assumed that the dielectric constant within the well and the barrier is the same. Using the momentum/energy-dependent momentum-relaxation time, the mobility of 2D electron gas is given as

$$\mu = \frac{e}{4\pi\hbar^2 N_s k_B T}\int_0^\infty \frac{E\tau(E)}{cosh^2\left[\frac{E-E_f}{2k_BT}\right]}dE, \tag{103}$$

where N_s is the 2D carrier concentration in the interconnect and is given as

$$N_s = g_v\frac{m_{DOS}k_BT}{\pi\hbar^2}log\left[1+exp\left(\frac{E-E_f}{k_BT}\right)\right], \tag{104}$$

where g_v is the valley degeneracy.

The scattering matrix element $|M(q)|^2$ is described next for various scattering mechanisms within the quantum well.

3.3.3.1 Acoustic deformation potential scattering

For acoustic deformation potential, the result of $|M(q)|^2$ from [130] is used. The mathematical expression for $|M(q)|^2(ADP)$ is given as

$$|M(q)|^2(ADP) = \frac{D_A^2 k_B T}{4\pi c_l}\int_{-\infty}^{\infty} F_f(z')F_i*(z')dz'\int_{-\infty}^{\infty} F_f(z')F_i^*(z')dz' = \frac{D_A^2 k_B T}{2c_l}\frac{1}{W_{fi}}, \tag{105}$$

where D_A is the acoustic phonon deformation potential, c_l is the longitudinal elastic constant, $F_f(z)$ and $F_i(z)$ are the envelope wavefunctions for the incident and scattered

electron waves. For an infinite, square well, the envelope wavefunctions are sine functions. Hence, W_{fi} is given as

$$\frac{1}{W_{fi}} = \frac{2+\delta_{fi}}{2W}, \tag{106}$$

where δ_{fi} is unity for $i = f$ and zero otherwise. For intra-subband scattering, the index i and f are identical. Therefore, $1/W_{fi} = 3/W$. At high temperatures, when screening can be neglected, the momentum-scattering rate due to acoustic phonons can be simplified to

$$\frac{1}{\tau_p^{ADP}(k)} = \frac{3m_z D_A^2 k_B T}{2\rho\hbar^3 u_l^2} k, \tag{107}$$

where ρ is the material density, u_l is the speed of longitudinal acoustic phonons. Neglecting screening, the mobility due to acoustic phonons in the 2D quantum well can be expressed as

$$\mu_{ADP} = \frac{2e\rho\hbar^3 u_l^2 W}{3m_{DOS}^2 D_A^2 k_B T}. \tag{108}$$

In Figure 60, the ADP-limited mobility in a 7.5 nm wide GaAs QW is plotted at R.T. as a function of the carrier concentration. Also shown are the ADP-limited mobilities for both GaAs bulk and for GaAs QWs upon ignoring screening of the scattering potential due to the presence of 2DEG. The mobility is underestimated upon neglecting screening particularly for high carrier concentrations.

We have compared the results of single-subband transport model with the experimental data obtained by Inoue & Matsuno [91] at 77K and 300K as shown in Figure 61. The difference between the results of the theoretical model and the experimental data increases with an increase in the well width. This is borne out of the fact that our theoretical model assumes a simplistic model for the wavefunctions confined within an infinite potential well, whereas, in reality, the penetration of the wavefunctions within the barrier increases with an increase in the well width.

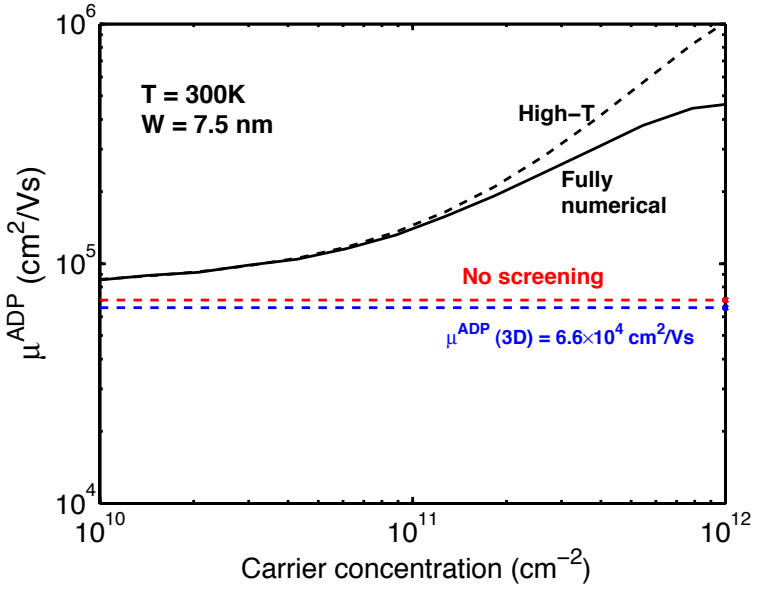

Figure 60: The dependence of ADP-limited mobility in GaAs QWs on the carrier concentration.

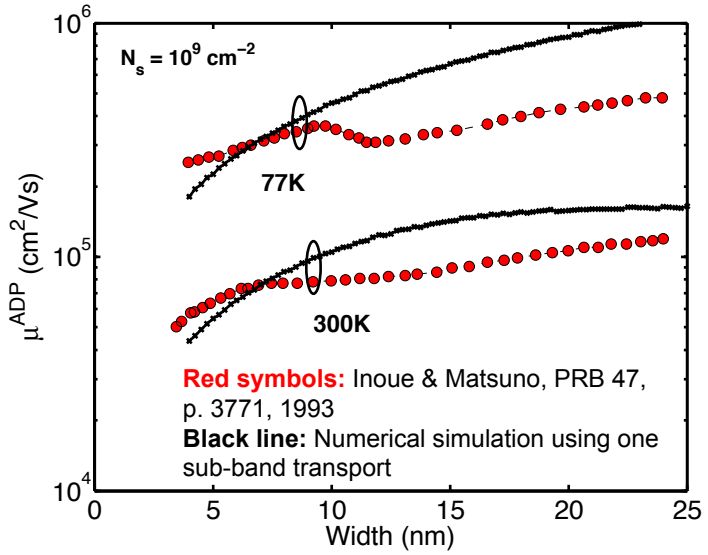

Figure 61: Mobility dominated by acoustic phonons as a function of the interconnect width at 300K and 77K. The dashed line with symbols is the numerical simulation result from Inoue and Matsuno [91]. The solid line with symbols corresponds to the approximate numerical result of Eq. (108).

3.3.3.2 *Ionized impurity scattering*

There are two kinds of doping profiles that are typically considered: (i) background doping and (ii) remote doping (see Figure 62). In this work, only the mobility limited due to electron scatterings from background doping is considered.

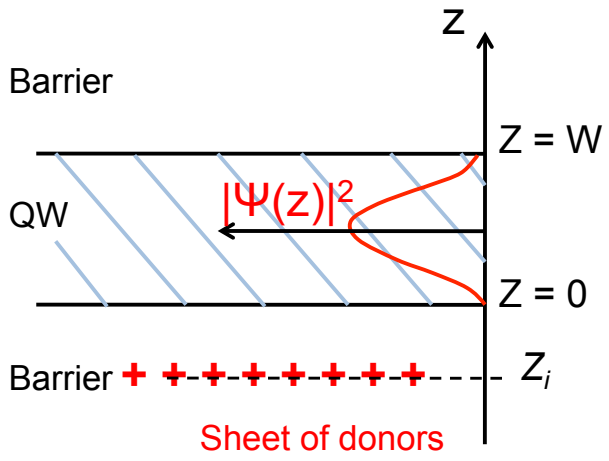

Figure 62: Configuration of a single QW with a sheet of donors.

The matrix element of electron scattering caused by background doping is given as

$$|M(q)|^2(II) = \left(\frac{2\pi e^2}{\kappa_0 q}\right)^2 \int N_{IMP}(z) F_I(q,z)^2 dz, \tag{109}$$

where N_{IMP} is the volume density of impurities and $F_I(q,z)$ is a form factor related to the electric field of ionized background impurities and is obtained by solving the electrostatic equation within the quantum well and the substrate and is mathematically given as

$$|M(q)|^2(II) = \left(\frac{2\pi e^2}{\kappa_0 q}\right)^2 N_{IMP} F_B(qW), \tag{110a}$$

$$F_B(x) = \frac{4}{x^2} + \frac{2x^2}{(x^2+4\pi^2)^2} - \frac{96\pi^4}{x^3(x^2+4\pi^2)^2}(1-e^{-x}) - \frac{128\pi^4}{x(x^2+4\pi^2)^2}(1-e^{-x}) + \frac{32\pi^2}{x^2(x^2+4\pi^2)^2}e^{-x}. \tag{110b}$$

Figure 63 shows the mobility in a 7.5 nm wide GaAs QW limited due to background impurity scatterings as a function of carrier concentration at R.T. As the impurity scattering potential is screened at high carrier concentrations, μ^{II} increases with an increase in carrier concentration.Impurity scatterings may limit the net mobility in QWs especially when N_{IMP} is high. Therefore, quantum wells are generally modulation doped so that the interaction between the electron and impurity wavefunctions can be reduced.

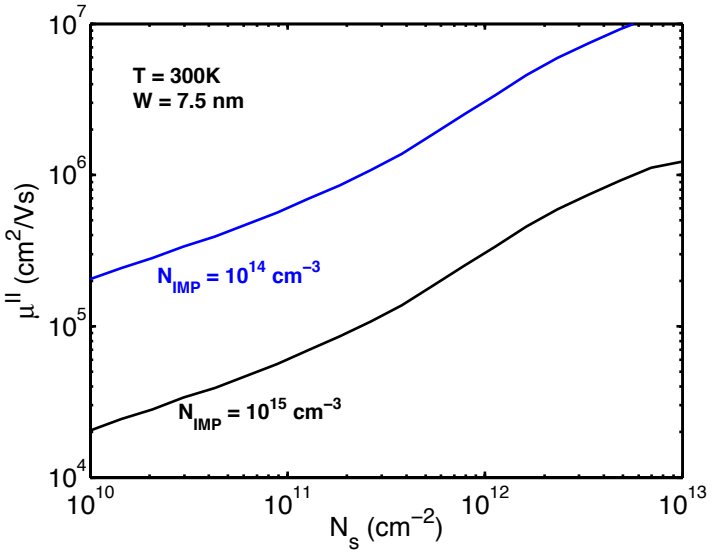

Figure 63: Mobility in GaAs QWs limited by ionized-impurity scatterings as a function of electron concentration at 300K for $N_{IMP} = 10^{14}$ cm^{-3} and 10^{15} cm^{-3}.

3.3.3.3 Interface roughness scattering

The interface roughness leads to a spatial variation in the width of the quantum well and consequently a variation in the confinement energies of the electron. The variation in the confinement energy acts as a fluctuating potential for the confined carriers leading to their scattering. The fluctuating potential is given as

$$\delta V(r) = \frac{\partial E_1}{\partial W}\Delta(r), \tag{111}$$

where E_1 denotes the first quantized energy level within the quantum well. The corresponding scattering matrix element is given as

$$|M(q)|^2(\text{IFR}) = \left(\frac{\delta E_1}{\delta W}\right)^2 S(q), \tag{112}$$

where $S(q)$ is the Fourier transform of the autocorrelation function of the well-width fluctuations. $S(q)$ depends strongly on the growth conditions of the quantum well. There are two kinds of autocorrelation functions that are typically discussed in literature: gaussian autocorrelation and exponential autocorrelation. For gaussian autocorrelation,

$$S(r) = \int \Delta(r' - r)\Delta(r')d^2r' = \Delta^2 e^{-r^2/\Lambda^2}, \tag{113}$$

where Δ is the average height of the well-width fluctuations, and Λ is the correlation length. The Fourier transform $S(q)$ for this autocorrelation function is given as

$$S(q) = \pi\Delta^2\Lambda^2 e^{-q^2\Lambda^2/4}. \tag{114}$$

The exponential autocorrelation function and the corresponding Fourier transform are given as

$$S(r) = \Delta^2 e^{-2\sqrt{r}/\Lambda}, \tag{115}$$

$$S(q) = \pi\Delta^2\Lambda^2 \left(1 + q^2\Lambda^2/2\right)^{-3/2}. \tag{116}$$

The inverse of the correlation length Λ^{-1} corresponds to an effective cut-off wavevector for the momentum exchange q. Using Eqs. (112) and (114), $|M(q)|^2(\text{IFR})$ for Gaussian autocorrelation can be simplified to

$$|M(q)|^2(\text{IFR}) = \frac{\pi^5\hbar^4\Delta^2\Lambda^2}{m_z^2 W^6} e^{-q^2\Lambda^2/4}. \tag{117}$$

If screening is neglected, the IFR-limited mobility in 2D quantum wells with Gaussian autocorrelation can be expressed as

$$\mu^{\text{IFR}} = \frac{15e m_z^2 W^6 \Lambda (k_B T)^{3/2}}{2^{3/2}\pi^4\hbar^4\Delta^2 m_{\text{DOS}}^{1/2}}. \tag{118}$$

From the above equation, it can be seen that the IFR-limited mobility may have a significant effect in semiconductors for which m_z/m_{DOS} is close to unity. In the case of GaAs, $m_z/m_{DOS} = 1$, while in the case of (001)-oriented silicon QW, $m_z/m_{DOS} << 1$. The mobility limited by interface-roughness scatterings for a 7.5 nm GaAs quantum well is shown in Figure 64 as a function of the correlation length. The average height of the well-width fluctuations is assumed to be 0.5 nm and the carrier concentrations are taken to be 10^{11} cm^{-2} and 10^{12} cm^{-2}. The IFR-limited mobility in QWs exhibits a minimum point with respect to the correlation length. For a well width of 7.5 nm, it is found that at a correlation length of 3-4 nm, the IFR-limited mobility is minimized for both Gaussian and exponential autocorrelation functions. The IFR-limited mobility increases with the correlation length for a correlation length that is $>> 1$ nm, and the IFR-limited mobility increases with a decrease in correlation length for correlation length that is $<< 1$ nm. Thus, it can be concluded that scattering by interface roughness is most efficient when the lateral scale of the roughness is of the same order as the electron wavelength.

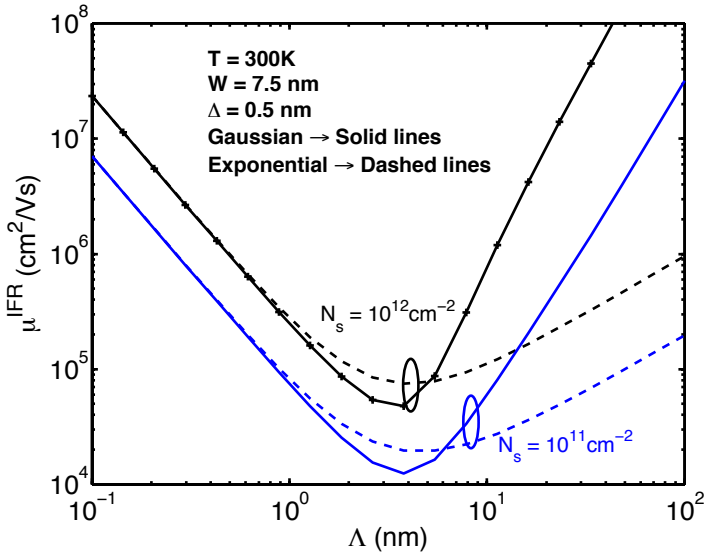

Figure 64: The impact of correlation length on the IFR-limited mobility of a 7.5 nm wide GaAs quantum well. The height of the fluctuations in the well width is assumed to be 0.5 nm.

Figure 65 shows how the IFR-limited mobility in GaAs QWs scales with the well width. The IFR-scattering limited mobility in GaAs QWs is found to scale as $W^{5.5}$ for both Gaussian and exponential autocorrelation functions. If screening were neglected, then μ^{IFR} would exhibit W^6 dependence on well width.

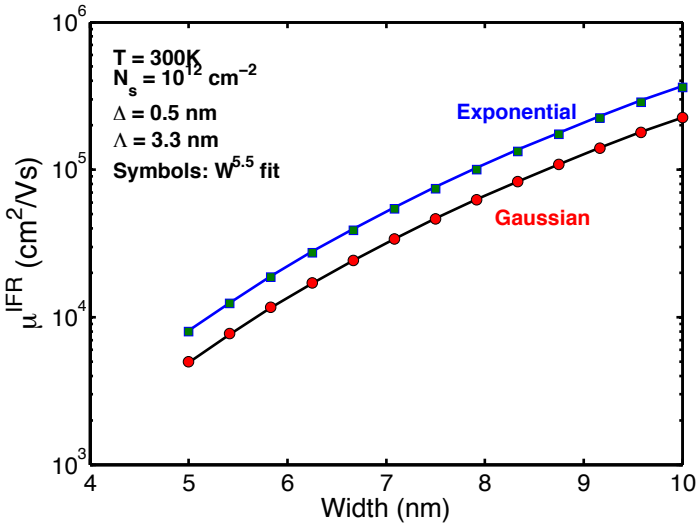

Figure 65: IFR-limited mobility in GaAs QWs versus well width at 300K using a fully-numerical approach for both Gaussian and exponential autocorrelation functions.

3.3.3.4 Optical phonon scattering

The scattering of electrons by polar optical phonons is especially important for III-V semiconductors near room temperature. Most studies conducted in the past to evaluate the momentum-relaxation rate for electron and polar-optical-phonon (POP) scattering in semiconductors used the assumption that the phonon spectrum in the quasi-2D quantum well is the same as that of the bulk. Even with this simplifying assumption, one has to ultimately resort to numerical techniques to calculate the POP momentum-relaxation time owing to the failure of momentum conservation approximation (MCA) for POP scattering. This is because POP scattering is largely an inelastic process that is accompanied with the absorption and emission of high

energy phonons. It was shown by exhaustive numerical and experimental results by Inoue and Matsuno, 1993 [91] that around room temperature, the mobility governed by POP scatterings is independent of GaAs well width for widths greater than 5 nm. For a silicon doping level of 2×10^{18} cm^{-3} in $Al_xGa_{1-x}As$/GaAs/$Al_xGa_{1-x}As$ (x=0.27), the experimental results on electron mobility in GaAs as a function of the well width as obtained by Inoue and Matsuno are shown in Figure 66. It can be seen from this figure that at room temperature, the dominant scattering mechanism in the quantum well is due to polar optical phonons. However, the phonon-dominated mobility for 2D and 3D structures is identical for well widths greater than 5 nm. An exhaustive quantitative study by Riddoch and Ridley, 1983 [184] also showed that the impact of 2D phonon spectra on the mobility of electrons in quasi quantum wells is negligible. Thus, one can conclude that the phonon-limited mobility is not strongly dependent on the two-dimensionality of the system, i.e., the well width. Hence, the model for POP-limited mobility in 2D quantum wells is assumed to be the same as that in bulk, with a POP-limited mobility of 9400 cm^2/Vs at 300K. At 77K, the dominant scattering mechanism that limits the electron mobility in the quantum well is due to ionized impurities.

The POP-limited mobility model for the GaAs QW can be given as

$$\mu^{POP} = 9400 \left(\frac{300}{T}\right)^{2.1} (cm^2/Vs). \tag{119}$$

3.3.3.5 Net mobility in GaAs QWs

Using the mobility models developed above for various scatterings mechanisms, the net mobility of GaAs quantum wells can be given by Mattheissen's rule according to

$$\frac{1}{\mu^{NET}} = \frac{1}{\mu^{ADP}} + \frac{1}{\mu^{II}} + \frac{1}{\mu^{IFR}} + \frac{1}{\mu^{POP}}. \tag{120}$$

The net mobility in GaAs QWs as a function of the well width is plotted in Figure 67 at R.T. It can be seen from this figure that the net mobility is dominated by polar

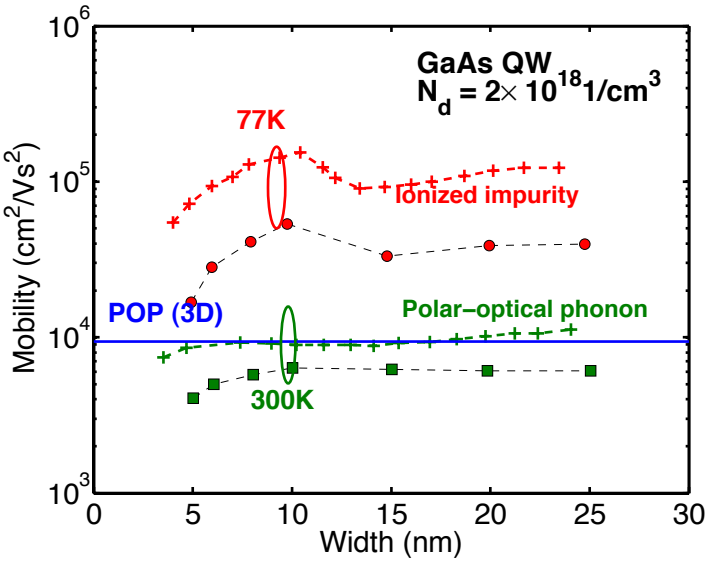

Figure 66: Mobility versus well width for GaAs quantum wells at 300K and 77K as obtained in [91]. The dotted lines with symbols are theoretical estimates by Inoue and Matsuno at 300K and 77K. The silicon doping concentration for the experiment is 2×10^{18} $1/cm^3$.

optical phonon scattering for well widths greater than 10 nm. Only when the well width is less than 5 nm, the IFR scatterings will also begin to limit the net mobility in the QWs. Also the theoretical model matches well with the experimental data obtained by Inoue & Matsuno [91].

The electron diffusion coefficient, D, in a 2D system is related to the electron mobility, μ, according to

$$\frac{\mu}{eD} = \frac{1}{k_B T} \frac{1}{F_0\left(\frac{E_f - E_1}{k_B T}\right)} \frac{1}{1 + exp\left(-\frac{E_f - E_1}{k_B T}\right)}, \tag{121}$$

where F_0 is the Fermi-Dirac integral of order zero. Figure 68 shows the diffusion coefficient versus the well width in GaAs at R.T. The electron diffusion coefficient increases with an increase in carrier concentration because of the screening of scattering potential by the 2DEG in the quantum well. The electron diffusion coefficient is > 100 cm^2/s for $W > 7$ nm at $N_s = 10^{11}$ cm^{-2}. The electron diffusion coefficient becomes greater than 300 cm^2/s for $W > 7$ nm for $N_s = 10^{12}$ cm^{-2}.

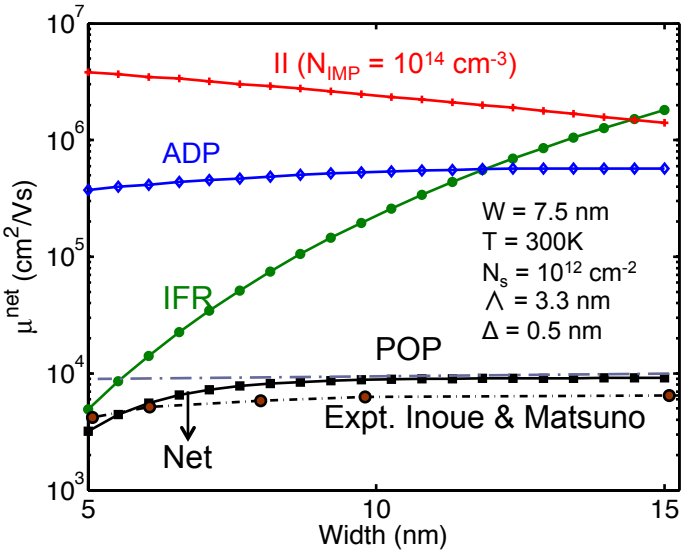

Figure 67: The net mobility of GaAs QW as a function of well width. The red symbols correspond to the experimental values of mobility obtained in [91].

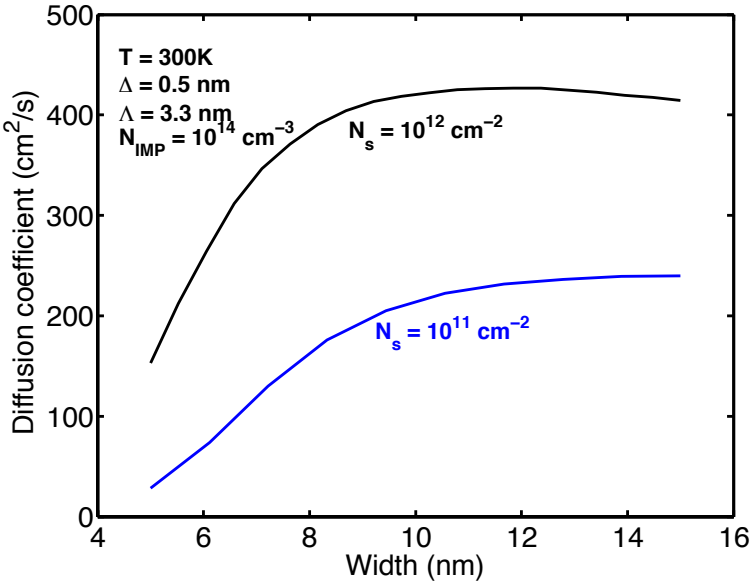

Figure 68: Electron diffusion coefficient in GaAs QWs versus interconnect width.

The electrical conductivity of the 2D electron gas in a quantum well is given using the Einstein's relation according to

$$\sigma = e^2 D \frac{\partial N_s}{\partial E_f}, \tag{122}$$

where N_s is the 2D carrier concentration. Using Eqs. (104) and (121), the conductivity is expressed in terms of the electron mobility according to

$$\sigma = \mu\,(ek_BT)\left(\frac{m_{DOS}}{\pi\hbar^2}\right)F_0\left(\frac{E_f - E_1}{k_BT}\right). \tag{123}$$

Figure 69 shows the electrical conductivity in a 2D GaAs quantum well as a function of the well width at R.T. The 2D conductivity degrades as the well-width scales below 10 nm particularly for low carrier concentration.

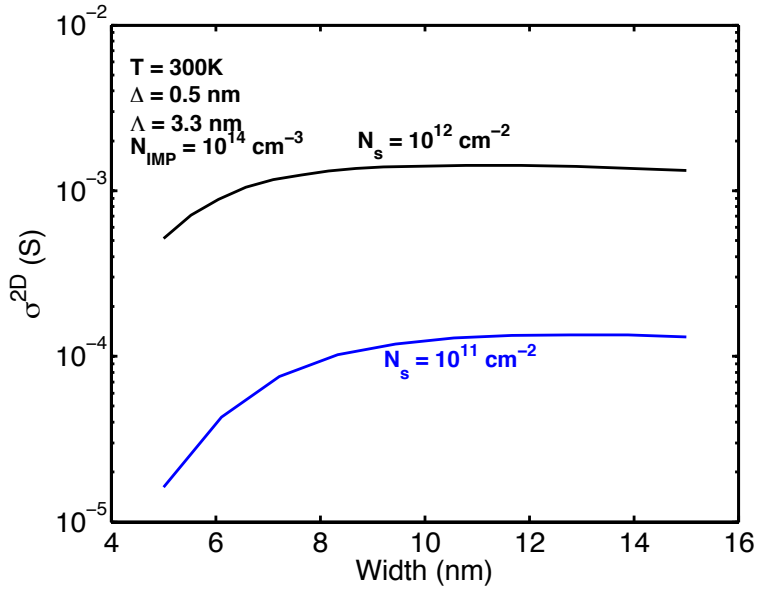

Figure 69: The 2D conductivity of electron gas in GaAs quantum well versus the well width at 300K.

3.4 Conclusions

In this chapter, physical models of the transport parameters that govern the performance and the energy dissipation of spin interconnects are presented. The impact of geometrical scaling and edge effects on the transport parameters are examined for a variety of interconnect materials: copper, aluminum, single- and multi-layer graphene nanoribbons, silicon, and gallium arsenide. The advantages of graphene that can be obtained from its long electron mean free path can only be materialized if graphene

can be patterned into nanoribbons with smooth edges. It is shown that even a 20% edge-scattering probability of electrons reduces the conductivity of graphene by an order of magnitude. Other transport parameters also degrade in the presence of edge roughness.

Metallic conductors such as aluminum and copper may be attractive for use as short spin interconnects particularly due to their ease of fabrication with matched-resistivity interface with injecting nanomagnet in spin-valve circuits. Even though the impact of size effects in metallic conductors is less severe than in graphene nanoribbons, it is shown that the resistivity of metallic conductors may increase by an order of magnitude or more in the presence of grain-boundary scatterings. Semiconducting interconnects offer the advantages of a mature technology with the flexibility of tuning the electrical properties of the material through doping to serve as both the interconnect and the device in a spin-logic fabric. For GaAs interconnects at narrow dimensions, quantum confinement effects are incorporated to obtain the transport parameters. It is found that interface roughness scattering may be the dominant scattering mechanism only at low temperatures and low doping concentrations. At around room temperature, scattering of electron by polar optical phonons in GaAs dominates for interconnects wider than 10 nm.

Table 20 summarizes the findings of this chapter. The values of spin transport parameters are provided for various interconnect materials. The interconnect width is taken to be 7.5 nm and the lattice temperature is assumed to be 300K. The best-case conductivity values are obtained for graphene nanoribbons. However, quantum resistance at the contacts must be incorporated for graphene nanoribbons to obtain the net resistance. The best-case carrier diffusivity is offered by graphene nanoribbons, while the lowest value of electron diffusivity is obtained for metallic conductors. The best-case electron mobility value is obtained for gallium arsenide quantum wells.

Table 20: Transport parameters in various spin interconnect materials. R denotes the grain-boundary reflectivity, p denotes the sidewall specularity. P_{GNR} is the edge-scattering coefficient, and E_f is the Fermi energy in the GNR. The c-axis resistivity in the case of ML-GNRs is taken to be 0.3 Ωm. For GNRs, the sheet resistance is quoted instead of the resistivity. N_d is the n-type doping in semiconducting interconnects. Values are quoted for interconnect width of 7.5 nm. Λ is the correlation length of the interface roughness, Δ is the height of the well-width fluctuations, and N_s is the sheet carrier density in the quantum well. The lattice temperature T = 300K.

Material	**Resistivity (Ω.m)**	**Diffusivity** (cm^2/s)	**Mobility** (cm^2/Vs)
Copper ($R = 0.5, p = 0$)	2×10^{-7}	3	17
Aluminum ($R = 0.5, p = 0$)	1.3×10^{-7}	2.7	20
Single-layer GNR ($P_{GNR} = 0.2, E_f = 0.4$ eV, λ_{sub} = 300 nm)	411 Ω	157.8	802
Multi-layer GNR ($P_{GNR} = 0.2, E_f = 0.4$ eV, N=4, L = 10 μm, λ_{sub} = 300 nm)	117	157.8	802
Silicon ($N_d = 10^{18}$ cm^{-3})	2.79×10^{-4}	7.5	275
Gallium Arsenide ($N_d = 10^{18}$ cm^{-3})	6.8×10^{-5}	90	2700
Gallium Arsenide QW ($\Lambda = 3.3$ nm, Δ = 0.5 nm, $N_s = 10^{11}$ cm^{-2})	7.92×10^{3} Ω	217	7836

CHAPTER IV

SPIN RELAXATION

Spin relaxation refers to the process by which a non-equilibrium population of electron spins is brought to its equilibrium value in a material. If an electron suddenly changes its spin orientation then it is referred to as "spin flip". However, if a spin population changes gradually with time then it is referred to as "spin relaxation". The aim of this chapter is to study spin-relaxation mechanisms relevant in non-magnetic interconnect materials and to obtain physical models of spin-relaxation length in these materials as a function of the interconnect width and size-effect parameters. The main cause of spin relaxation is the spin-orbit coupling (SOC) that arises due to various intrinsic and extrinsic effects in materials. It is SOC that in conjunction with momentum relaxation of electrons gives rise to the relaxation of electron spins. From classical electrodynamics, in the rest frame of the electron, the proton is circling around it. The circling proton has a current and a magnetic field associated with it. The magnetic field exerts a torque on the magnetic dipole moment of the spinning electron causing a change in its quantized energy by an amount Δ_{so}, also called the SOC. This eventually causes the non-equilibrium population of electron spins to relax to its equilibrium value. The main spin relaxation mechanisms due to various spin-orbit couplings in materials can be broadly categorized into the following:

Elliott-Yafet (EY) In most materials that are centrosymmetric (metals and group-IV semiconductors), this is the dominant spin-relaxation mechanism. According to the EY spin-relaxation mechanism, there is a finite probability of spin flip associated with every momentum-scattering event. Thus, the net spin-relaxation time is proportional to the momentum-relaxation time.

D'yakonov-Perel' In the case of III-V semiconductors like GaAs, bulk-inversion asymmetry leads to a lift-off of spin degeneracy. This is known as the Dresselhaus spin-orbit coupling (DSOC). The effective magnetic field due to DSOC causes electrons to precess about the magnetic field. The angle by which spins rotate between consecutive momentum-relaxation events is $\phi = \Omega_k \tau_p$, where τ_p is the momentum-relaxation time, and Ω_k is the momentum-dependent precession frequency. In a random-walk model, the variance after N time steps is $< \phi >^2 = < \Omega_k >^2 \tau_p^2 N$. Electron spins are assumed to have relaxed when the mean-squared angle after N steps is large. Assuming spins relax when $< \phi >^2 \sim 1$, the number of time steps required for this is $N = \tau_s/\tau_p$, which gives $< \Omega_k >^2 \tau_p \tau_s \sim 1$. Hence, according to the D'yakonov-Perel (DyP) mechanism, $\tau_s \propto \tau_p^{-1}$.

Bir-Aronov-Pikus This mechanism is a source of spin relaxation in p-type semiconductors. In this case, the electron is in close proximity with holes. Thus, the wave functions of the electrons and holes overlap, which causes an exchange interaction between them. The exchange interaction leads to eventual spin relaxation in p-type semiconductors.

Hyperfine interaction This interaction refers to a magnetic interaction between the magnetic moments of the nuclei and electrons. It is relatively of little importance at R.T. in bulk semiconductors and metals, but may become important to consider in the case of electrons confined in quantum dots or for donor-bound electrons.

4.1 Techniques to measure spin relaxation

In this section, we focus on two commonly used techniques to measure spin-relaxation time in materials.

4.1.1 Conduction electron spin resonance (CESR)

The first technique is the conduction electron spin resonance (CESR), which provides rich information about the electron-phonon and electron-impurity interactions through the signal intensity and the power absorption line-width. From the data on the measured line-width (ΔB), the spin-relaxation time, τ_s, is obtained according to

$$\alpha \frac{1}{\tau_s} = \gamma \Delta B, \tag{124}$$

where $\gamma = g\mu_B/\hbar$ is the gyromagnetic ratio of the electron, and α is a factor of the order of unity that depends on the observed line shape of the absorption spectra. For a sample thinner than the skin depth, $\alpha = 2$, while for a thicker sample, a Dysonian line shape is used to fit the data. In the latter case, the value of α depends upon the ratio of the skin depth and the spin-relaxation length. When the spin-relaxation length dominates, then $\alpha \approx 1$[1].

4.1.2 Spin valve signal

There are typically two kinds of spin-valve structures that are used to measure the spin-relaxation length (see Figure 70). The first is a three-terminal (3T) spin-valve structure in which one of the ferromagnetic electrodes is common between the injection and the detection terminals. By contrast, in a four-terminal (4T) spin-valve structure, there are no common ferromagnetic electrodes between the injection and the detection terminals. In either of the spin-valve structures, an electrical injection of spin-polarized electrons is accomplished from the ferromagnet into the non-magnetic channel. As the spin-polarized electrons diffuse spatially, another ferromagnetic contact is used to detects the amount of spin through the Johnson-Silsbee coupling. By fitting the spin signal at the receiver using an exponential function of the form $e^{-L/Ls}$, where L is the length through which the electron spins have diffused, the

[1]For a complete theory of possible line shapes of the absorption spectra of the CESR, refer to [54].

spin-relaxation length, L_s, in the non-magnetic channel can be extracted.

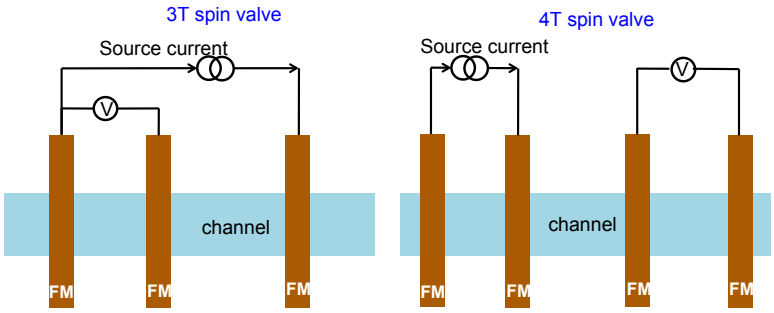

Figure 70: The left figure shows a three-terminal spin valve, while the right figure is a four-terminal spin valve (also called a non-local spin valve).

4.2 Metallic conductors- Cu and Al

In centrosymmetric materials such as metals and group-IV semiconductors, the dominant spin-relaxation mechanism is known as the Elliott-Yafet (EY) mechanism. In 1954, Elliott [58] showed that the existence of a spin admixture together with a spin-independent scattering potential could lead to the spin relaxation of conduction electrons. The spin-orbit coupling, V_{so}, induced by the periodic potential, V_{sc}, of the lattice ions, i.e. phonons is given as

$$V_{so} = \frac{\hbar}{4m^2c^2}\nabla V_{sc} \times \hat{p}.\hat{\sigma}, \tag{125}$$

where m is the free electron mass, $\hat{p}$ is the linear momentum operator ($=-i\hbar\nabla$), and $\hat{\sigma}$ are the Pauli spin matrices. In the presence of spin-orbit coupling, the electronic Bloch states are an admixture of spin-up and spin-down states. The Bloch states are represented as

$$\Psi_{\bar{k}n\uparrow}(\bar{r}) = [a_{\bar{k}n}(\bar{r})|\uparrow> + b_{\bar{k}n}(\bar{r})|\downarrow>]\, e^{i\bar{k}.\bar{r}}, \tag{126}$$

$$\Psi_{\bar{k}n\downarrow}(\bar{r}) = \left[a^*_{-\bar{k}n}(\bar{r})|\downarrow> - b^*_{-\bar{k}n}(\bar{r})|\uparrow>\right] e^{i\bar{k}.\bar{r}}. \tag{127}$$

The states corresponding to $\Psi_{\bar{k}n\uparrow}(\bar{r})$ and $\Psi_{\bar{k}n\downarrow}(\bar{r})$ are degenerate and can be chosen to represent electrons polarized along the z-direction; this is because in most cases

the typical value of $|a|$ is close to unity and that of $|b|$ is much less than unity. Hence, these states can still be labeled as up- and down-spin states, respectively. The probability of an electron spin flipping at any momentum scattering event is $\approx |b|^2$. That is, $\tau_p/\tau_s \approx < |b^2| >$, where τ_p is the momentum-relaxation time, τ_s is the spin-relaxation time, and $< |b^2| >$ is obtained by averaging the value of $|b^2|$ over the entire Fermi surface. In the case when bandstructure non-idealities are removed and it is assumed that only one band contributes significantly to the spin-orbit coupling, it can be shown that $|b| \approx (\lambda_{so}/\Delta E)$, where λ_{so} is the amplitude of the matrix element of spin-orbit interaction between the two coupled states, and ΔE is the energy difference between the considered band and the nearest band that is coupled to it via the spin-orbit coupling. However, this estimate of $|b| \approx (\lambda_{so}/\Delta E)$ works well for monovalent metals like Cu and Ag but fails for polyvalent metals like Al. Elliott showed that the relationship between τ_s and τ_p is given as

$$\frac{1}{\tau_s} = (\Delta g)^2 \frac{1}{\tau_p}, \tag{128}$$

where Δg is the deviation of the g-factor of conduction electrons from their free-electron value ($g_0 = 2.0023$). Several CESR experiments have been conducted to obtain τ_s and empirically test the validity of the Elliott relation in metals. The experimental technique of CESR is more suited to establishing a relationship between τ_s and τ_p because it avoids the need of an ambiguous parameter $(\lambda_{so}/\Delta E)$. When the Elliott relation for spin relaxation due to phonons in metals was empirically tested by Beuneu and Monod in 1978 [21], they found that most metals obeyed the law

$$\frac{1}{\tau_s} \propto \frac{(\Delta g)^2}{\tau_p}, \tag{129}$$

where the constant of proportionality lies between one and 10. Table 21 shows the values of Δg and (τ_p/τ_s) due to phonons for various metals. The data was collected by Beuneu and Monod, 1978.

Table 21: Values of Δg for metals and the ratio of momentum-relaxation time and spin-relaxation time. Data collected by Beuneu and Monod, 1978.

Material	Δg	τ_p/τ_s
Cu	$(3.1\pm0.1)\times10^{-2}$	$\approx (\Delta g)^2 = 10^{-3}$
Al	$(-5\pm1)\times10^{-3}$	$\approx 10 \times (\Delta g)^2 = 1.6 \times 10^{-5}$
Ag	$(-1.9 \pm 0.1) \times 10^{-2}$	$\approx 10 \times (\Delta g)^2 = 3.6 \times 10^{-3}$
Au	(0.1 ± 0.01)	$\approx 10 \times (\Delta g)^2 = 0.01$

In 1963, Yafet [242] showed that the product of the temperature-dependent spin-relaxation rate, $\Gamma_s(T)$, and the temperature-dependent material resistivity, $\rho(T)$, is a constant. That is, $\Gamma_s(T)\rho(T) = C$, where the constant of proportionality, C, depends on the presence of band-structure anomalies such as *spin hot spots*, particularly in the case of polyvalent metals like aluminum [253], [62]. In 1978, it was shown by Meservey and Tedrow [145] that the conduction-electron-spin scattering at a metal surface is caused by the spin-orbit interaction. Hence, similar to the case of spin relaxation due to phonons, the relationship between the spin-relaxation time and the momentum-relaxation time due to surface defects can be expressed as $\tau_p/\tau_s = C'$, where the constant, C', is a function of the atomic number of the metal under consideration. Hence, a generalized EY relation for the spin relaxation in metals is proposed as

$$\left(\frac{\tau_p}{\tau_s}\right)^i = a^i = f\left(\eta_{so}^i\right), \tag{130}$$

where the index i corresponds to the i^{th} scattering mechanism, and η_{so}^i is the corresponding spin-orbit coupling. For phonon-induced scatterings, a^{ph} is equal to 10^{-3} in Cu and 1.2×10^{-4} in Al, as obtained from CESR measurements and also by theoretical calculations using realistic pseudoptentials in the case of polyvalent Al by Fabian and Das Sarma [62]. In the absence of magnetic impurities in the sample, Mattheissen's rule can be used to combine the spin-relaxation times due to various scatterings to obtain the net spin-relaxation time. That is,

$$\frac{1}{\tau_s^{net}} = \frac{1}{\tau_s^d} + \frac{1}{\tau_s^{ph}}. \tag{131}$$

Equation (131) can be simplified using Eq. (130) to give

$$\frac{1}{\tau_s^{net}} = \frac{\tau_p^d \tau_p^{ph}}{\tau_p^d \alpha^{ph} + \tau_p^{ph} \alpha^d}. \tag{132}$$

The net spin relaxation length, $L_s^{net} = \sqrt{D\tau_s^{net}}$ can be simplified to give

$$L_s^{net} = \frac{\lambda^d \lambda^{ph}}{\sqrt{3\left(\lambda^d + \lambda^{ph}\right)\left(\alpha^{ph}\lambda^d + \alpha^d \lambda^{ph}\right)}}. \tag{133}$$

In this research work, the values of the constants α^d and α^{ph} are extracted from experimental data on the spin-relaxation length from spin-valve experiments as described in Section 4.1.2. Figure 71 shows the spin-relaxation length in Cu versus the material conductivity taken from various experiments using the non-local spin-valve (NLSV) geometry at 4.2K and 300K. At 300K, the best-case spin-relaxation length in Cu is less than 500 nm, for material conductivities between (0.3-0.5) $\mu\Omega.cm$ for all the samples. At 4.2K, when all the phonon modes are adequately frozen, the spin-relaxation length in Cu is between 500 nm-1 μm. In the case of Al, the best-case spin-relaxation length reported with NLSV experiments is 600 nm at 300K and 1200 nm at 4.2K (Figure 72).

To experimentally extract the value of α^d and α^{ph} from experimental results, the following expressions are used:

$$\alpha^d = \frac{1}{3}\left(\frac{m^* v_f}{e^2 n_{3D}\left(\rho L_s\right)_{4.2K}}\right)^2, \tag{134}$$

$$\alpha^{ph} = \frac{1}{3}\left(\frac{m^* v_f}{e^2 n_{3D}\left(\rho L_s\right)_{300K}}\right)^2, \tag{135}$$

where m^* is the effective mass of electrons in the metal, v_f is the Fermi velocity of electrons, n_{3D} is the three-dimensional carrier concentration in the material, and the product ρL_s is known from the experimental data. Using the above relations, the experimentally extracted values of α^d and α^{ph} for Cu are plotted in Figure 73. The value of α^{ph} lies between $(1-2)\times 10^{-3}$, while α^d lies between $(2-7)\times 10^{-4}$. These values show that SOC induced due to phonons in Cu is stronger than that introduced due to defects.

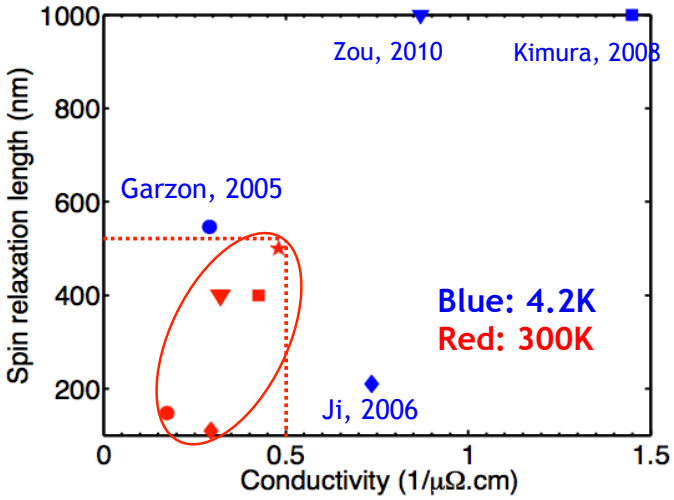

Figure 71: Spin-relaxation length, L_s, in Cu versus the material conductivity at 4.2K and 300K. Only data points from non-local spin-valve geometry have been considered. Data extracted from [95], [69], [112], [251], [236], [93], [94].

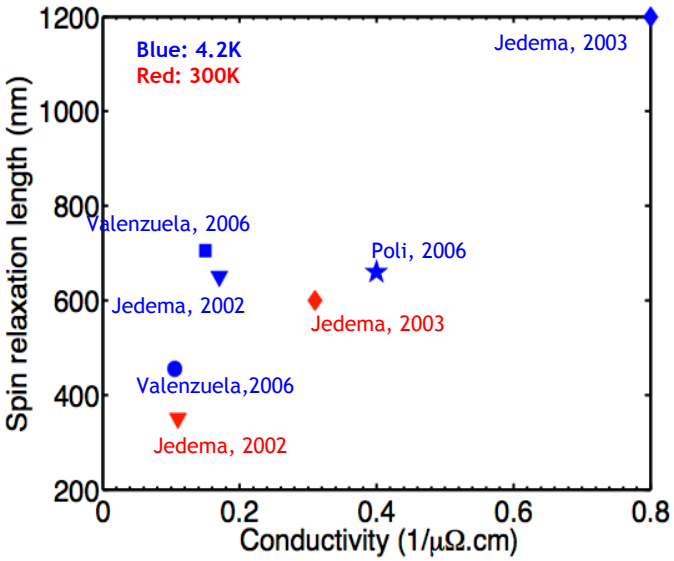

Figure 72: Spin relaxation length, L_s, in Al versus the material conductivity at 4.2K and 300K. Only data points from non-local spin-valve geometry have been considered. Data extracted from [92], [93], [163], [227].

For simulations, the values selected for α^d and α^{ph} are 7.3×10^{-4} and 2×10^{-3} from Jedema et al. [93]. From Figure 73, it can be seen that a few experiments yield significantly larger values of α^d (Ji et al. and Kimura et al.). The reason for

these larger values is the presence of extrinsic factors that open up additional spin-relaxation channels in these samples. In the case of the sample studied by Y. Ji et al., there are magnetic impurities in the sample that "increase the spin-flip scattering per scattering event" [94]. For the sample studied by Kimura & coworkers [112], the reason noted by the authors in the work for lower values of spin-relaxation time without any substantial increase in resistivity is that their Cu sample has oxidized surfaces. The oxidized regions "provide stronger spin-flip scatters than the inside of the Cu layer."

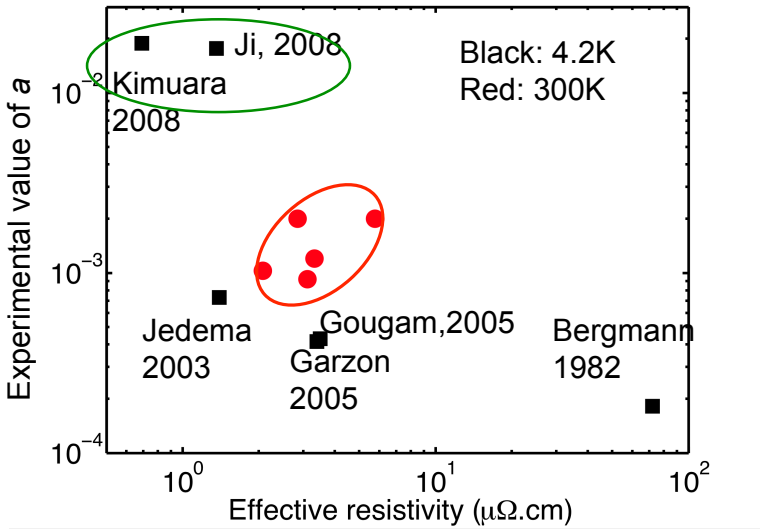

Figure 73: Experimentally extracted value of α versus the effective resistivity of Cu. The value of α extracted at 4.2K corresponds to α^{d}, while the value extracted at 300K corresponds to α^{ph}.

The value of α extracted from NLSV experiments in Al versus its effective resistivity is plotted in Figure 74. For simulations, the values selected for α^{d} and α^{ph} are 3.7×10^{-4} and 1.3×10^{-4} from Jedema et al [93]. The value of α^{ph} in Al as extracted from experiments is much larger than the value obtained from using the atomistic calculations. The reason for this is that aluminum being a polyvalent metal has spin hot-spots on its Fermi surface. If an electron spin jumps from or into a spin hot

spot, the spin flips with a much higher probability. However, the value of α^{ph} in Al is still lesser than that in Cu, signifying that relaxation of electron spins mediated by phonons is slower in Al than in Cu.

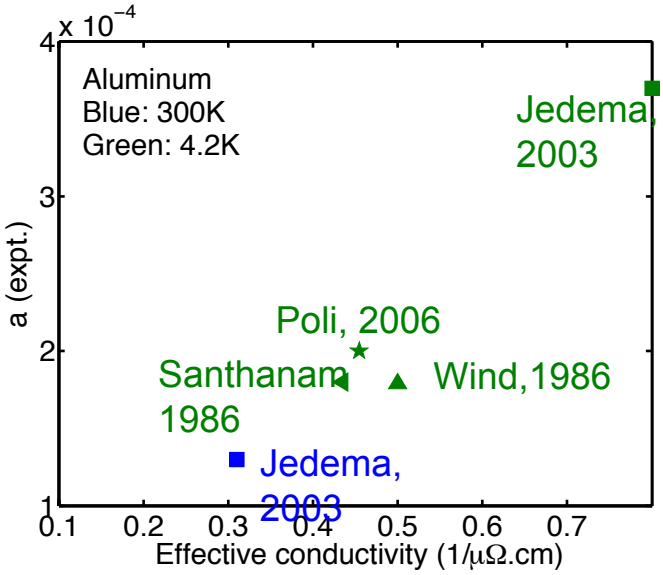

Figure 74: Experimentally extracted value of α versus the effective resistivity of Al. The value of α extracted at 4.2K corresponds to α^{d}, while the value extracted at 300K corresponds to α^{ph}.

To evaluate the spin-relaxation length in metals, the knowledge of λ^{d} and λ^{ph} is needed in addition to the knowledge of α^{d} and α^{ph}. Figure 75 shows the value of the effective MFP of electrons versus the grain-boundary reflectivity of Cu and Al interconnects. The vertical green line in Figure 75 corresponds to a grain-boundary reflectivity $R = 0.145$ and specularity $p = 0$. The value $R = 0.145$ is extracted from Cu NLSV experiments in [93] (see Chapter III). The value of p was assumed to be zero. This is because Rosnagel and Kuan reported that Cu/Ta interface should be diffusive for electrons due to the fact that the Fermi surafces of Cu and Ta do not match yielding a very low value of specularity at the sidewalls [186]. Hence, for the extraction of R from experiments, p was assumed to be between 0 and 0.2. For a 10 nm wide Cu interconnect, the effective MFP of electrons is 8.3 nm at $R = 0.145$ and

$p = 0$. For the same values of R, p, and W, the defect-induced MFP of electrons in Cu is found to be 10.5 nm. In the case of Al, the value of R extracted from Al NLSV experiments is 0.01 at $p = 0$ [93]. This gives an effective electron MFP of 5 nm and a defect-induced electron MFP of 7 nm in Al for a 10 nm wide interconnect.

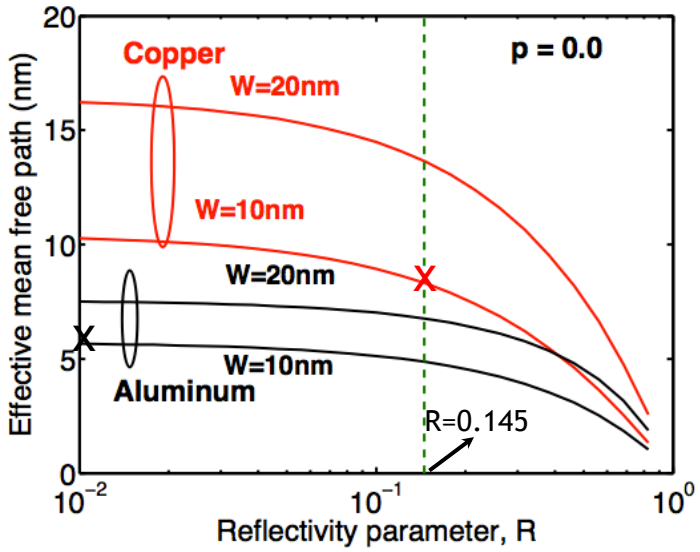

Figure 75: Effective MFP of electrons in Cu and Al versus the grain-boundary reflectivity of the interconnect. Two values of the interconnect width are selected: W = 10 nm and W = 20 nm.

The spin-relaxation length in Cu and Al at R.T. is plotted in Figure 76 versus the interconnect width. In the absence of size effects, the spin-relaxation length in Al is 0.62 μm, while that in Cu is 0.5 μm. This is because the spin-orbit-coupling energies due to phonons and defects in Al are lower than that in Cu. Without any size effects, the spin-relaxation length in metals is independent of the interconnect width. At $R = 0.145$ and $p = 0$, the spin-relaxation length in Cu degrades to 154 nm for a 10 nm wide interconnect. At $R = 0.01$ and $p = 0$, the spin-relaxation length in Al degrades to 258 nm at W = 10 nm.

The impact of sidewall specularity on the spin-relaxation length in Cu and Al is plotted in Figure 77 in the absence of any grain-boundary reflectivity ($R = 0$). The

spin-relaxation length in Al is greater than that in Cu irrespective of the sidewall specularity parameter at $R = 0$ and W=10 nm. This is again attributed to the lower spin-orbit coupling in aluminum than in copper.

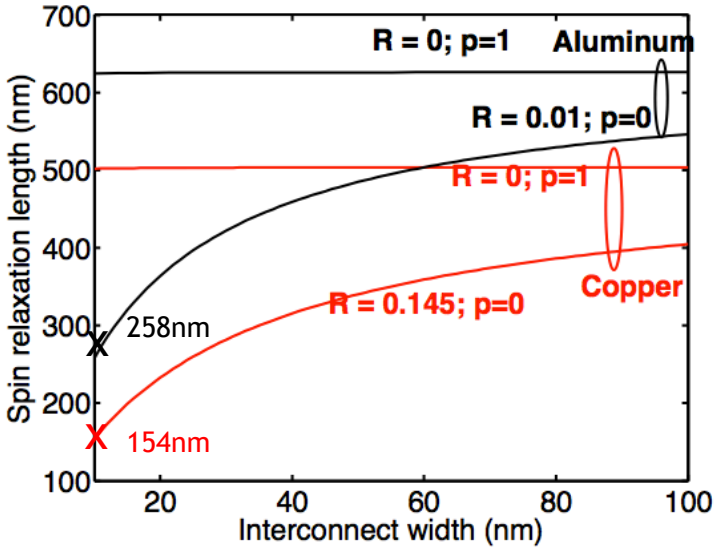

Figure 76: Spin relaxation length at R.T. in Cu and Al versus interconnect width.

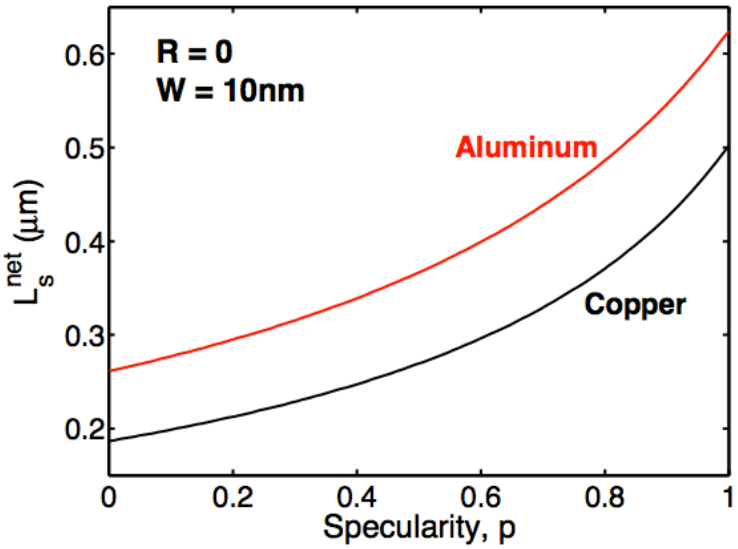

Figure 77: Spin-relaxation length at R.T. in metals as a function of sidewall specularity. Interconnect width is assumed to be 10 nm and no grain-boundary reflections are assumed.

4.3 Graphene

Graphene has a low atomic number $Z = 6$; hence, it has a lower intrinsic spin-orbit coupling, which suggests a much longer spin-relaxation length than that in metals. The main SOCs that need to be considered for graphene on a substrate are (i) atomic, (ii) ripple-induced, and (iii) substrate-induced (remote phonons and charge impurities). The various SOCs in graphene, Δ_{so}, are tabulated in Table 22.

Table 22: Various spin-orbit couplings in graphene. N_{imp} denotes the impurity concentration. The curvature-induced coupling constant, Δ_{so}^{curv} depends on the ripple radius, which has been assumed to be between 50-100 nm. The value for substrate-induced τ_s is quoted for a Fermi energy, $E_f = 0.1$ eV. All values are at R.T. unless otherwise noted.

Coupling constant	**Value (eV)**	τ_s	**Reference**
Δ_{so}^{int} (intrinsic)	8.6×10^{-7}	18 μs	[88]
Δ_{so}^{curv} (curvature)	1.7×10^{-5}	0.28 μs	[88]
Δ_{so}^{sub} (substrate)	7.24×10^{-8}	0.6 ms	[59]
($N_{imp} = 4 \times 10^{11} 1/cm^2$)			
Δ_{so}^{sub} (substrate)	2.17×10^{-6}	6 μs	[59]
($N_{imp} = 4 \times 10^{12} 1/cm^2$)			

In the case of graphene, the atomic SOC is relatively weak because of the low atomic number of carbon ($Z = 6$). However, owing to its corrugated surface, there is always going to be an inherent ripple-induced SOC in graphene. The ripples in graphene have a coupling strength that is 20× stronger than the intrinsic coupling in graphene. The substrate-induced SOC depends on the concentration of charged impurities existing at the interface between the graphene sheet and the substrate and the distance between the graphene sheet and the substrate ($\approx$ 0.35 nm). The presence of polar phonons and charged impurities in the substrate lead to what is called a

Bychkov-Rashba (BR) SOC, which manifests itself as a momentum-dependent magnetic field around which electron spins tend to undergo precession. The effective precession frequency is given as $\Omega_{eff} = 2\zeta_{BR}E_{eff}/\hbar$, where E_{eff} is a momentum-averaged effective electric field perpendicular to the sample plane, and ζ_{BR} is a BR coupling constant. The values of ζ_{BR} from rough estimate is 0.258 μeV/V/nm [103]; from tight-binding model, ζ_{BR} is estimated to be 17.9 or 66.6 μeV/V/nm [82], [149]; from first-principles calculation, ζ_{BR} is found to be 5 μeV/V/nm [59]. The theoretically-estimated values of τ_s in graphene for various SOCs are provided in Table 22.

Here we provide a quantitative estimate of the spin-relaxation time in graphene. Such an estimate is useful in highlighting the fundamental limitations of using graphene as the channel material in ASL. A generalized form of spin-relaxation time in graphene using Mattheissen's rule is given as [77]

$$\frac{1}{\tau_s} = \frac{K^{EY}}{\tau_p} + K^{DyP}\tau_p, \tag{136}$$

where the factors K^{EY} and K^{DyP} result from either the EY-type or the DyP-type scaling, respectively, of spin-relaxation time with momentum-relaxation time, τ_p. It has been shown in [201], [59], [244], [158] that for various scattering mechanisms K^{EY} can be approximated as $(\Delta_{so}^{eff}/E_f)^2$, where E_f is the Fermi energy; K^{DyP} is approximated as $(\Delta_{so}^{eff}/\hbar)^2$. Δ_{so}^{eff} is an effective SOC that includes the effect of ripples in graphene, impurities and phonons in the substrate, and edge roughness for narrow GNRs, and also adatoms for dirty graphene samples. The net spin-relaxation time will follow a DyP scaling when $(K_f\lambda^{eff})^2 >> 1$, where K_f is the Fermi wavevector. In the DyP regime, the spin-relaxation length is independent of the electron MFP.

In Figure 78, the spin-relaxation time in bulk graphene is plotted as a function of the carrier concentration. The landscape of τ_s versus N_s exhibits a maximum point at which the spin-relaxation mechanism changes from EY to DyP. The value of τ_s at this maximum point is approximately 90 ns. The inset plot of Figure 78 shows the spin-relaxation length versus carrier concentration in bulk graphene at R.T.. As

the DyP mechanism dominates for carrier concentrations in excess of 10^{12} cm^{-2}, the spin-relaxation length saturates to approximately 20 μm. This is a typical signature of the DyP mechanism, where L_s is no longer a function of the electron MFP.

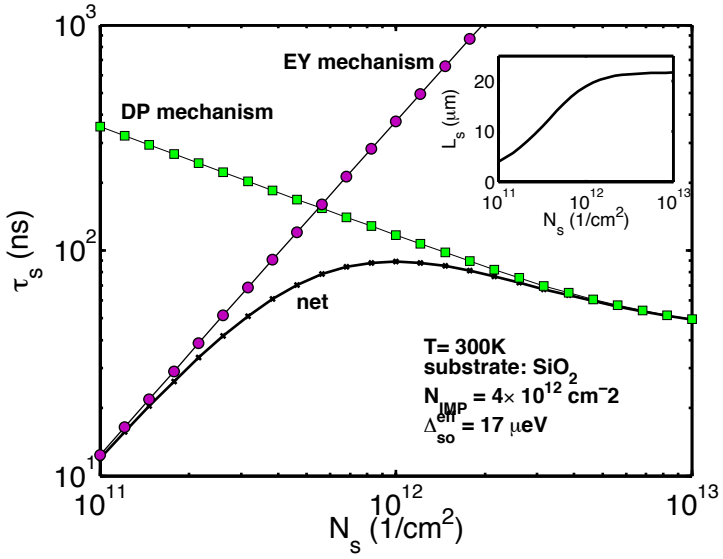

Figure 78: Spin-relaxation time versus carrier concentration in bulk graphene. The inset plot shows the spin-relaxation length versus carrier concentration,

In Figure 79, the spin-relaxation length in graphene nanoribbons is plotted as a function of the ribbon width for various values of the spin-orbit coupling, Δ_{so}^{eff}. The spin-relaxation length is nearly constant for ribbons with width more than 10 nm. For Δ_{so}^{eff} dominated by curvature-induced coupling in graphene, the value of L_s for W >10 nm and E_f = 0.2 eV and P_{GNR} = 0.2 is approximately 17 μm. The spin-relaxation length degrades quadratically with an increase in Δ_{so}^{eff} such that for Δ_{so}^{eff} = 0.1 meV, L_s saturates to 2.9 μm for W > 10 nm . The impact of edge roughness on L_s is only minimal as seen in the inset plot of Figure 79, which is again a typical characteristic of the DyP spin-relaxation mechanism.

A survey of spin-relaxation lengths in graphene from spin-valve experiments is shown in Table 23 given at the end of this section. The experimentally measured L_s at R.T. is between (1-2) μm in most cases; these values are an order of magnitude

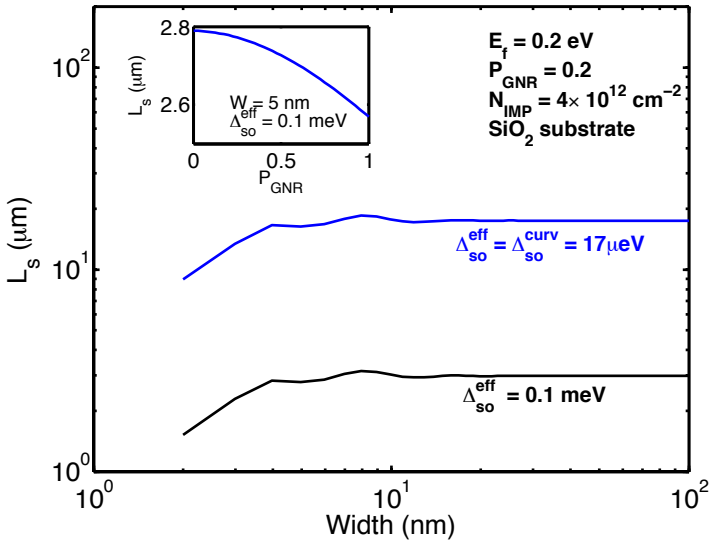

Figure 79: Spin-relaxation length in GNR versus ribbon width. The inset plot shows the impact of edge-scattering coefficient on the spin-relaxation length of a 5 nm ribbon.

lower than the theoretically estimated values even upon considering substrate-induced spin relaxation in graphene. Further, there is considerable debate in literature on the relationship between the spin-relaxation time and the momentum-relaxation time in graphene. When τ_s is proportional to momentum-relaxation time τ_p, it is more commonly referred to as EY-type spin relaxation, while for $\tau_s \propto \tau_p^{-1}$, it is identified as the DyP-type spin relaxation.

The Groeningen research group recently published experimental data that showed an EY-type spin relaxation to be present in graphene at all carrier densities [99]. However, the experimental results of the Riverside group shown an EY-type spin relaxation in graphene at 4K, while at R.T., the EY mechanism of spin relaxation could not explain their experimental findings [77]. Experimental observations on spin relaxation in graphene that seem to stem neither from intrinsic factors like curvature SOC nor extrinsic factors such as the substrate have been explained by multiple theoretical physicists by considering adatoms in graphene [164], [158]. If certain type of

adatoms that hybridize with the carbon atoms are present in graphene, they induce a localized spin-orbit coupling, $\Delta_{so}^{loc}(\mathbf{r})$, due to the distortion of the lattice coordination. This localized adatom SOC is typically several orders of magnitude larger than other SOCs in graphene due to inversion asymmetry and ripples. The experimental setup of spin valves to measure the spin-relaxation length unintentionally introduces metallic adatoms because of the close proximity of graphene channel with the ferromagnetic contacts. A thorough investigation of spin relaxation in graphene due to the random Rashba field (RRF) of the adatoms using kinetic spin Bloch equations (KSBE) was performed by Zhang and Wu in 2011 [244]. By fitting and comparing their theoretical results with experiments, they were able to conclude that the dominant spin-relaxation mechanism in the experimental results is the one due to the average Rashba field induced by adatoms, and the nature of this spin relaxation mechanism can change from DyP to EY depending on the environmental factors such as the electron density and the ambient temperature.

Table 23: A survey of experimental values of spin-transport parameters in single-layer graphene. The temperature is 300K unless otherwise stated. P_j denotes the injection efficiency.

Reference	**D** (cm^2/s)	$L_s(\mu m)$	τ_s **(ps)**	P_j	**W** (μm)
Shiraishi et al, 2009 [196]	210	1.6	120	0.09	-
Han and Kawakami, 2011 [77] (T=4K)	300	5.1	900	–	–
Han and Kawakami, 2011 [77]	130	2.4	447	–	–
Pi et al, 2010 [171]	200	1.48	110	–	–
Josza et al, 2009 [99]	160	1	62.5	–	0.3
Han et al, 2010 [78]	–	2	–	(0.2-0.31)	2
Han et al, 2009 [79]	120	1.5	84	0.013	1.9
Josza et al, 2009 [100]	200	2	200	0.18	0.5
Popinciuc et al, 2009 [173] ($n_e = 1.8 \times 10^{12} 1/cm^2$)	300	1.8	106	0.053	1.1
Popinciuc et al, 2009 [173] ($n_e \approx 0$)	180	1.4	100	0.04	1.1
Popinciuc et al, 2009 [173] ($n_e = 1.8 \times 10^{12} 1/cm^2$)	270	2	145	0.093	0.3
Popinciuc et al, 2009 [173] ($n_e \approx 0$)	130	1.1	92	0.074	0.3
Tombros et al, 2008 [224] ($n_e = 10^{12} 1/cm^2$)	200	0.8	21	–	1.2
Tombros et al, 2008 [224] ($n_e = 2 \times 10^{12} 1/cm^2$)	300	1	33	–	1.2

4.4 Silicon

It was shown by Yafet, 1963 [242] that for semiconductors in which the minimum of the conduction band is not at $k = 0$, the spin-relaxation time due to lattice vibrations is given as

$$\frac{1}{\tau_s^{ph}} = \frac{2}{\pi^{3/2}\hbar}\frac{D'^2}{\rho u^2}\frac{2m^* kT^{5/2}}{\hbar^2}, \tag{137}$$

where ρ is the material density, u is the velocity of sound, $D' \approx Ca\Delta g$, where a is the order of lattice constant, C is the deformation potential, and Δg is the difference in the g-factors of conduction electrons in silicon and free electrons. The Yafet relation in Eq. (137) shows that the temperature dependence of τ_s^{ph} in silicon is $T^{-5/2}$ if Δg is considered to be a temperature-independent parameter. Indeed, this temperature dependence has been used to fit experimental data, especially at low temperatures [87]. However, a study conducted in 1964 by Lancaster & coworkers [120] showed that the roll-off of τ_s^{ph} with temperature is steeper than $T^{-5/2}$. This temperature dependence is suggested to result from the interaction of electrons with both intra- and inter-valley acoustic phonons. The interaction between electrons and inter-valley acoustic phonons becomes more active for temperatures greater than 160K. Hence, a modification to the temperature dependence of spin-relaxation time due to phonons in silicon may be needed. To extract the temperature dependence of the spin-relaxation time in phosphorus-doped silicon (Si:P) more accurately from experiments, we use the data from Lepine, 1970 [123]. In 1970, Lepine studied the CESR of Si:P for temperatures between 50K and 300K. The doping of phosphorus in silicon was kept below 10^{17} cm^{-3} for all the samples studied by Lepine. In Figure 80, the CESR data collected by Lepine is fitted using $T^{-\theta}$ for various values of θ. It is found that $\theta = 3$ fits the data set most accurately for low-doping concentrations and T>150K. The choice of θ also matches with the theoretical estimate by Cheng et al. [36] and Restrepo & Windl [183]. The data collected by Lepine for T<150K is not shown,

since the spin-relaxation mechanism in silicon at low temperatures is not governed by the Elliott-Yafet mechanism but rather by the hyperfine interaction between electrons and phosphorus nuclei (donor-bound electrons) [123].

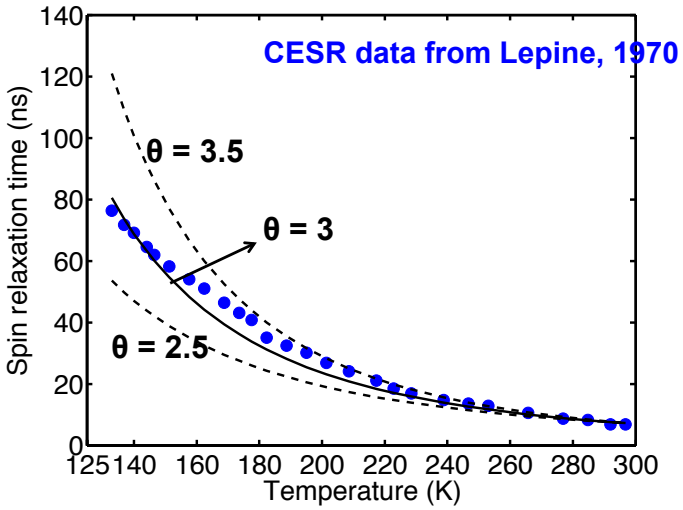

Figure 80: Spin-relaxation time in Si with a doping of 10^{14} cm^{-3} measured using CESR by Lepine, 1970 [123].

Based on the experimental fitting of Lepine's data as well as theoretical calculations, the following model for phonon-mediated spin-relaxation time, τ_s^{ph}, in silicon is suggested:

$$\tau_s^{ph} = \tau_0 \left(\frac{T}{300K} \right)^{-\theta}, \tag{138}$$

where τ_0 is the spin-relaxation time due to phonons at 300K and is equal to 7.7 ns, and $\theta = 3$.

The spin-orbit interaction due to impurities in silicon becomes especially important at high doping concentrations. In 1964, H. Kodera [114] obtained a theoretical relationship between the CESR line-width of non-degenerately-doped silicon and the impurity-dominated mobility. This relationship between ΔH and μ^{IMP} is given as

$$\frac{\Delta H}{(\Delta g)^2} = \frac{A(T)}{\mu_{IMP}}, \tag{139}$$

where Δg is the difference in the g-factors of the conduction electrons in silicon and free electrons, and $A(T)$ is a pre-factor that varies linearly with temperature and is doping independent. Using Eq. (124), the spin-relaxation time due to impurities, τ_s^{IMP}, can be given as

$$\frac{1}{\tau_s^{IMP}} = \alpha(T)\frac{1}{\mu^{IMP}}. \tag{140}$$

We define $\alpha(T) = \gamma A(T)\,(\Delta g)^2$. If Δg is independent of doping and temperature for non-degenerate doping in silicon, then $\alpha(T)$ will also be doping independent and will vary linearly with temperature. Figure 81 shows the values of Δg versus doping at 300K and 78K from experimental data collected by Graenacher and Czaja, 1967 (referred to as "GC, 1967" hereafter) [75]. It can be seen from Figure 81 that Δg is only slightly sensitive to doping for non-degenerate doping and varies only very slightly from T = 78K to T = 300K. Hence, the assumption that $\alpha(T)$ varies linearly with temperature and is doping-independent in silicon is justified.

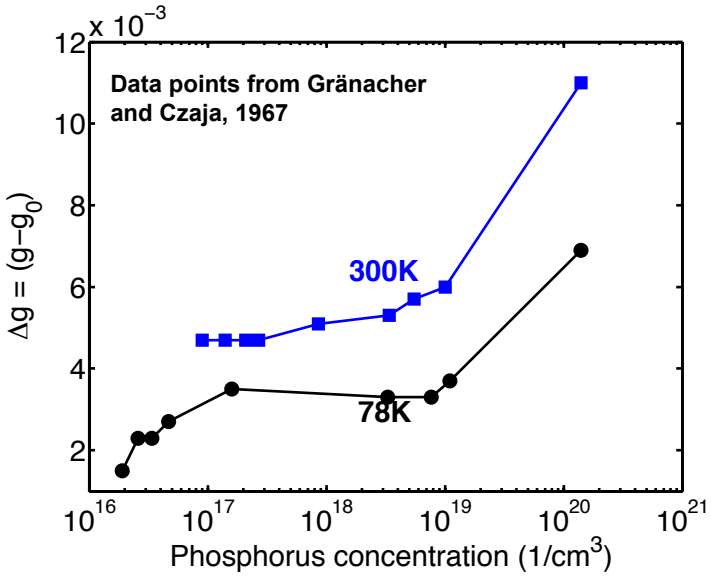

Figure 81: Δg versus the doping concentration in silicon at 300K and 78K. Data collected by Graenacher and Czaja, 1967 [75].

According to Eq. (140), the relationship between $1/\tau_s^{IMP}$ and $1/\mu^{IMP}$ is linear

at a given temperature. The slope of the plot of $1/\tau_s^{IMP}$ versus $1/\mu^{IMP}$ at a given temperature is equal to $\alpha(T)$ for that temperature. At 300K, the data on Hall mobility of Si:P from GC, 1967 is used to obtain $1/\mu^{IMP}$ using the Klaassen electron-mobility model in silicon. Then the data on τ_s is used to extract the contribution of impurities by removing the contribution of phonons to spin relaxation in silicon at R.T. (= 7.7 ns). Figure 82 shows the plot of $1/\tau_s^{IMP}$ versus $1/\mu^{IMP}$ at 300K by using data sets from GC, 1967 and H. Kodera, 1970 [116].

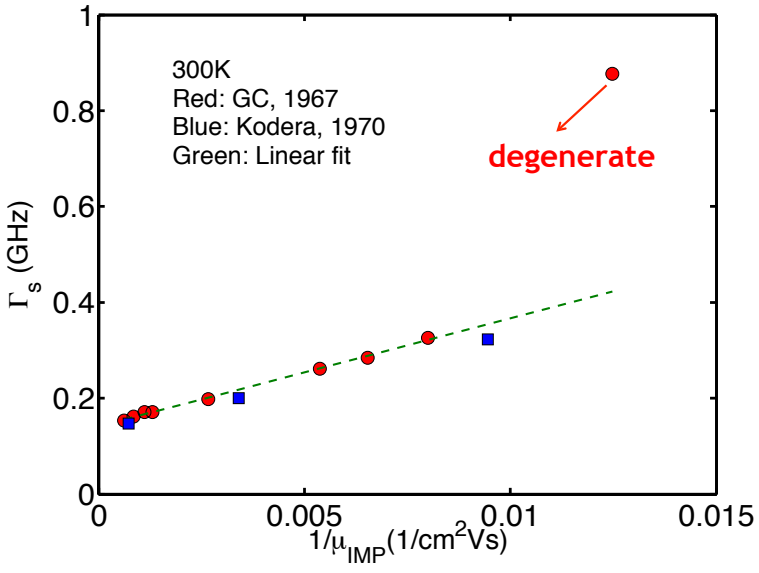

Figure 82: Spin-relaxation rate due to impurities versus the inverse of impurity-dominated mobility in silicon at 300K.

It can be seen from Figure 82 that the spin-relaxation rate due to impurities is linearly proportional to the inverse of the momentum-dominated mobility in silicon. The slope, which is $\alpha_0 = \alpha(300K)$, is extracted to be 2.249×10^{10} cm^2/Vs^2 at 300K. The linear relationship between $1/\tau_s^{IMP}$ and $1/\mu^{IMP}$ is not preserved at the temperature of 78K as can be seen from Figure 83. This result is attributed to the fact that at low temperature other spin-relaxation mechanisms might be more dominant than the Elliott-Yafet mechanism of spin relaxation. To further examine the choice of α_0, the

data from Suzuki & coworkers, 2011 [217] with a doping concentration of 5×10^{19} cm^{-3} is shown in Figure 84. The spin-relaxation time in Suzuki et al., was measured using a lateral non-local spin-valve device. Spin injection and Hanle-type spin precession signals were successfully measured at R.T. Using a value of $\alpha_0 = 5 \times 10^{10}$ cm^2/Vs^2 in our theoretical model of Eq. (140), the experimental data can be very well explained. The experimentally-measured spin-relaxation time data rolls off as T^{-2} with temperature. Our theoretical model predicts a slower temperature dependence, which is $\sim T^{-1.7}$.

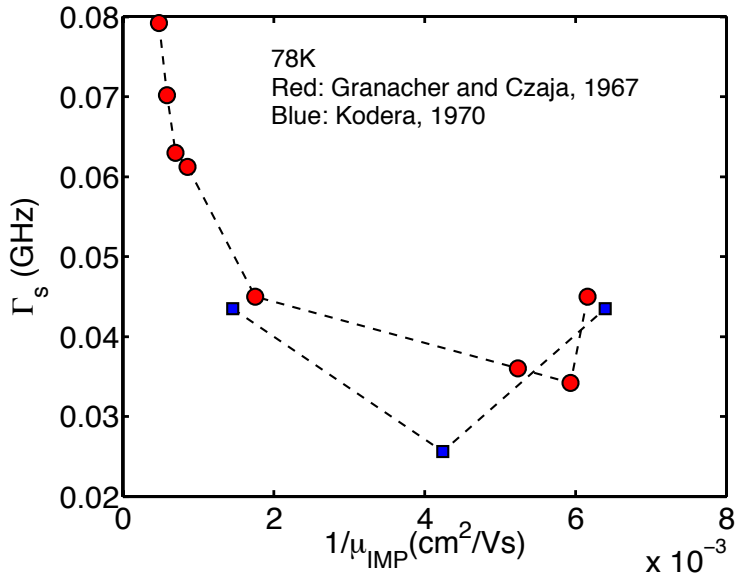

Figure 83: Spin relaxation rate due to impurities versus the inverse of impurity-dominated mobility in silicon at 78K.

From a rich source of experimental data using CESR in Si:P at low and high temperatures, the following semi-empirical model of spin relaxation in non-degenerately doped silicon for T≥150K is suggested:

$$\frac{1}{\tau_s} = \frac{\alpha_0\,[T/300K]}{\mu^{IMP}(T, N_d)} + \frac{1}{\tau_0\left(\frac{T}{300K}\right)^{-\theta}}, \tag{141}$$

where α_0, τ_0, and θ are fitting parameters. Their values have been extracted from experiments: $\alpha = 2.25 \times 10^{10}$ cm^2/Vs^2, $\tau_0 = 7.7$ ns, and $\theta = 3$.

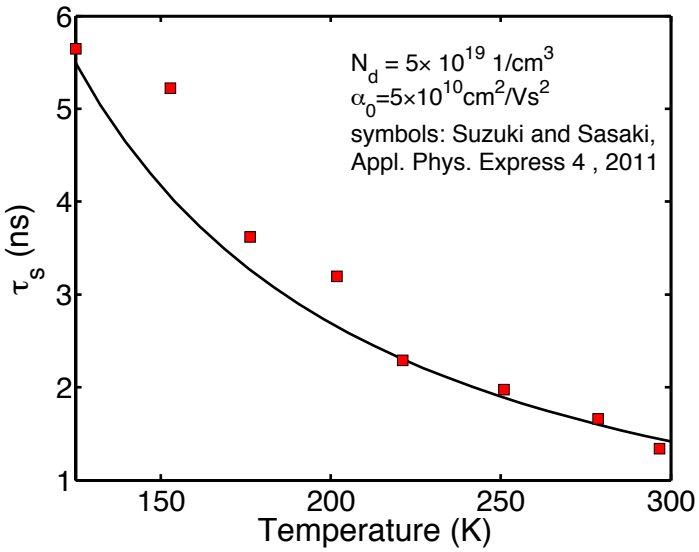

Figure 84: Temperature-dependent spin-relaxation time for a doping concentration of 5×10^{19} $1/cm^3$. Fitted with theoretical model of Eq. (140) with $\alpha_0 = 5 \times 10^{10}$ cm^2/Vs^2.

The complete spin-relaxation model in silicon is tested for a range of temperatures and doping concentrations using experimental data from Lepine, 1970 [123] and Kodera, 1969 [115]. The results are shown in Figures 85 and 86, respectively. The semi-empirical model of the spin-relaxation time in silicon matches very well with the experimental data for T>150K and doping $N_d \leq 10^{19}$ cm^{-3}. The error percentage between the results from the theoretical model and the experimental data is less than 10% at 300K for all doping levels less than 10^{19} cm^{-3}.

Using the semi-empirical spin-relaxation model developed for non-degenerately doped silicon, the spin-relaxation length versus doping in silicon at various temperatures is plotted in Figure 87. The room-temperature spin-relaxation length in Si degrades from 5 μm at $N_d = 10^{14}$ cm^{-3} to 1 μm at $N_d = 10^{19}$ cm^{-3}. At 200K, the degradation in the spin-relaxation length is from 12 μm to 1.2 μm as the doping increases from 10^{14} cm^{-3} to 10^{19} cm^{-3}, while at 400K the degradation in the spin-relaxation length is from 2.72 μm to 0.82 μm for the same change in the doping

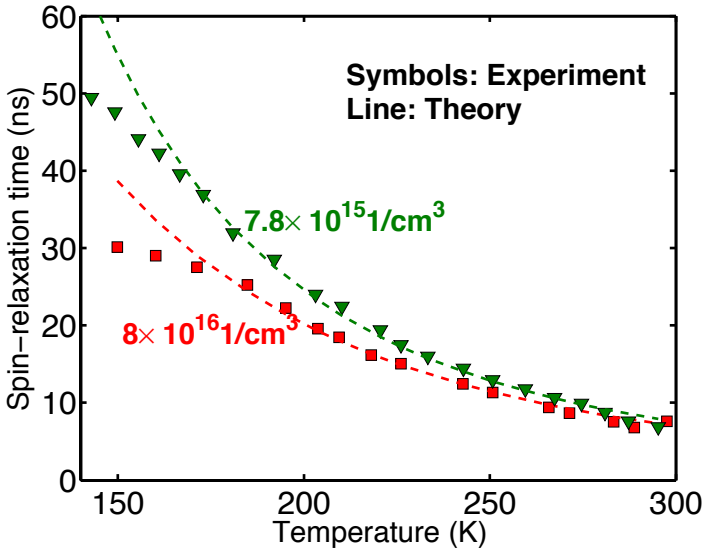

Figure 85: Spin-relaxation time versus temperature from theoretical model (dashed line) and from measured data by Lepine, 1970 [123] (symbols).

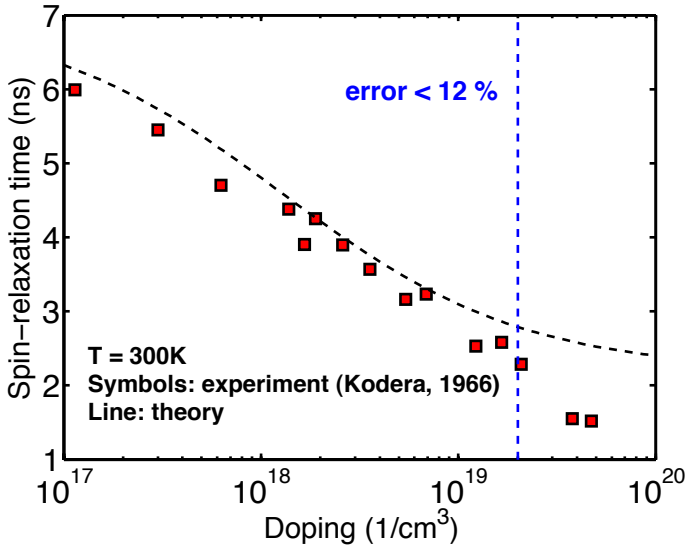

Figure 86: Room-temperature spin-relaxation time versus doping in silicon from theoretical model (dashed line) and measured data by Kodera, 1969 [115] (symbols).

density. Hence, the spin-relaxation length degrades more rapidly with an increase in doping concentration at low temperatures. The room-temperature spin-relaxation length in silicon at low-doping levels is approximately an order of magnitude larger

than the best-case spin-relaxation lengths obtained in Cu and Al. Even at high doping levels, the spin-relaxation length in silicon is higher than that in the case of metals.

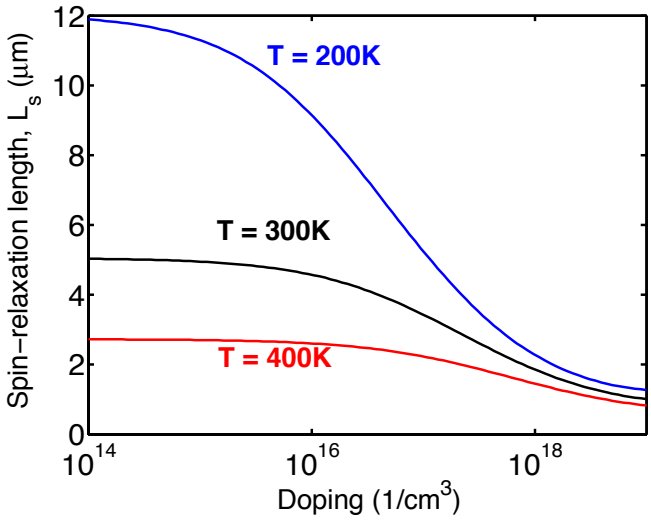

Figure 87: Spin-relaxation length versus doping concentration in silicon at various temperatures.

It is important to compare the results of CESR-measured spin-relaxation time with the results obtained using spin-valve measurements in silicon. The experimental data on spin-relaxation time measured by C.H. Li et al. [128] using a 3T spin-valve structure is provided in Table 24. A doping concentration of 10^{18} cm^{-3} is used in the experiment. The diffusion coefficient in silicon for various doping levels is obtained using the models described in Chapter III.

The coefficient $\alpha(T)$ extracted from the data in Table 24 as a function of temperature is shown in Figure 88. It is found that $\alpha(300K) = 5 \times 10^{11} cm^2/Vs^2$. This value is an order of magnitude larger than the value of $\alpha_0 = \alpha(300K)$ obtained from CESR data in Si:P. Further, the linear temperature dependence of $\alpha(T)$ around room temperature is not preserved in this experimental data. This discrepancy can be explained if one takes into account the impact of contact electrodes whose vicinity with the spin-current channel (the semiconductor) opens up additional spin-relaxation

paths and ultimately leads to a more rapid spin relaxation than in the bulk Si used in CESR experiments. The impact of contacts on the spin relaxation is more severe in the case of three-terminal geometries such that the usual ordering of spin-relaxation times measured using various experimental setups is $\tau_s(\mathrm{CESR}) > \tau_s(4\mathrm{T}) > \tau_s(3\mathrm{T})$.

Table 24: Data from C.H. Li et al. [128] on spin-relaxation length in silicon for a doping concentration of 10^{18} cm^{-3}. Diffusion coefficient has been obtained from the theoretical model described in Eq. (75) in Chapter III.

Temperature (K)	L_s (nm)	D (cm^2/s)	τ_s (ps)
10.8	121.67	0.93	158.76
49.9	151.45	1.13	202.78
101.0	209.27	1.75	250.42
153.52	237.12	2.48	226.98
201.9	381.09	3.18	456.03
251.5	410.9	3.92	430.71
300.8	386.24	4.60	324.31
327.9	434.81	4.96	381.41

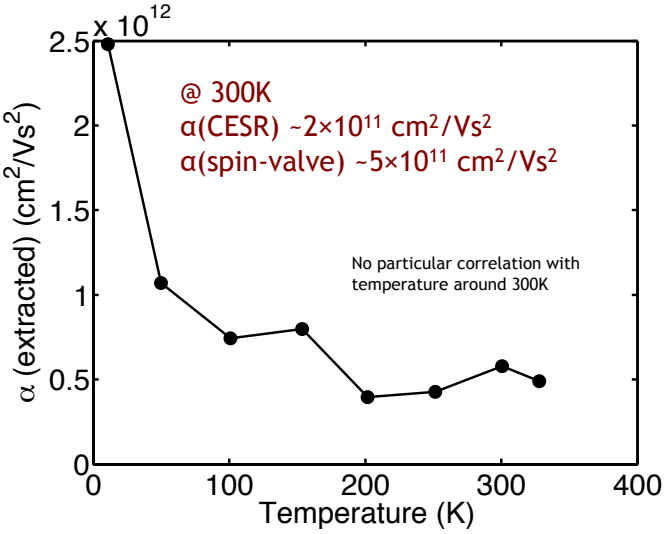

Figure 88: The value of $\alpha(\mathrm{T})$ extracted from 3T non-local spin-valve measurements from C.H. Li et al. [128].

4.5 Gallium Arsenide

Due to the lack of bulk inversion symmetry, the dominant spin-orbit interaction in GaAs is the Desselhaus spin-orbit interaction. Due to the presence of Dresselhaus spin-orbit coupling (DSOC), there exists an intrinsic momentum-dependent magnetic field, $B_i(k)$ in the crystal around which the electron spins undergo precession with a Larmor frequency, $\Omega(k) = e/mB_i(k)$. The momentum-dependent precession of electrons in conjunction with momentum relaxation (characteristic time τ_p) leads to spin dephasing. There are two limiting cases of spin dephasing due to DSOC: (a) $|\Omega|\tau_p << 1$ ("strong-scattering limit") and (b) $|\Omega|\tau_p >> 1$ ("weak-scattering limit"). The strong-scattering limit is also identified as the "motional-narrowing regime" of the D'yakonov-Perel' spin-relaxation mechanism. For the motional-narrowing regime DyP mechanism, the spin-relaxation time is inversely proportional to the momentum-relaxation time. In 1988, Pikus and coworkers [172] obtained the spin-relaxation rate in bulk GaAs as

$$\frac{1}{\tau_s(E_k)} = \frac{32}{105}\gamma_3^{-1}\tau_p(E_k)\alpha^2\frac{E_k^3}{\hbar^2 E_g}. \tag{142}$$

In the above equation, $\alpha = 2\gamma_D\sqrt{m_c^3 E_g}$, where m_c is the effective mass of conduction electrons, E_g is the band gap of GaAs, γ_D is the Dresselhaus spin splitting and is found to be (2.19-2.39)$\times 10^2$ eV/nm [165], [247]. This gives α between 0.063 and 0.07; α specifies the strength of the spin-orbit coupling. γ_3 depends on the dominant scattering mechanism; $\gamma_3 \approx 6$ for ionized-impurity scattering; $\gamma_3 \approx 1$ for acoustic-phonon scattering; $\gamma_3 \approx 41/6$ for polar optical phonon. E_k is the energy of the electron, and τ_p is the momentum-relaxation time of electrons. Strictly speaking, other spin-relaxation mechanims such as the EY mechanism or hyperfine interaction also exist in GaAs. However, around room temperature, it is indeed the DyP mechanism that is dominant [205].

For a degenerate electron gas, E_k in Eq. (142) is replaced with Fermi energy, E_f.

For a non-degenerate electron gas, thermal averaging of $\tau_s(E_k)$ over the Boltzmann distribution yields

$$\frac{1}{\tau_s^i} = Q^i < \tau_p >^i \alpha^2 \frac{(k_B T)^3}{\hbar^2 E_g}, \tag{143}$$

where the index i denotes the i^{th} scattering mechanism, $< \tau_p >=< \tau_p E_k > / < E_k >$ is the thermally-averaged momentum-relaxation time of the non-degenerate electron gas. The factor Q^i is given as

$$Q^i = \frac{16}{35}\gamma_3^{-1}\left(\nu^i + \frac{7}{2}\right)\left(\nu^i + \frac{5}{2}\right), \tag{144}$$

where ν^i is the power law of the momentum-relaxation time on energy ($\tau_p^i \sim E_k^{\nu^i}$). For ionized impurities, $Q \approx 1.5$; for piezoelectric or optical phonons, $Q \approx 0.8$; for acoustic-phonons, $Q \approx 2.7$. The Sotoodeh mobility model for GaAs is used to extract the momentum-relaxation time as a function of doping and temperature. The spin-relaxation time in bulk GaAs as obtained using the Sotoodeh mobility model is plotted in Figure 89 as a function of doping concentration at 300K. Also shown on this plot are the experimental data points from Bungay & coworkers [27] and Kimel & coworkers [111]. The experimental data points fit very well on the analytical curve for spin-relaxation time obtained using the Sotoodeh model in conjunction with the DyP theory for GaAs. An average value of $Q = 3$ is used for the simulation in Figure 89.

A distinguishing feature of the DyP spin-relaxation mechanism is that the spin-relaxation length is independent of the momentum-relaxation time. Hence, for a degenerate electron gas in GaAs, the spin-relaxation length is both independent of temperature and doping. In the case of a non-degenerate electron gas, the spin-relaxation length rolls of as T^{-1} with temperature. Hence, the spin-relaxation length in non-degenerately doped GaAs at any temperature may be given as

$$L_s(T) = L_0\left(\frac{T}{300K}\right)^{-1}, \tag{145}$$

where L_0 is the spin-relaxation length in bulk GaAs at room temperature, and it is independent of doping.

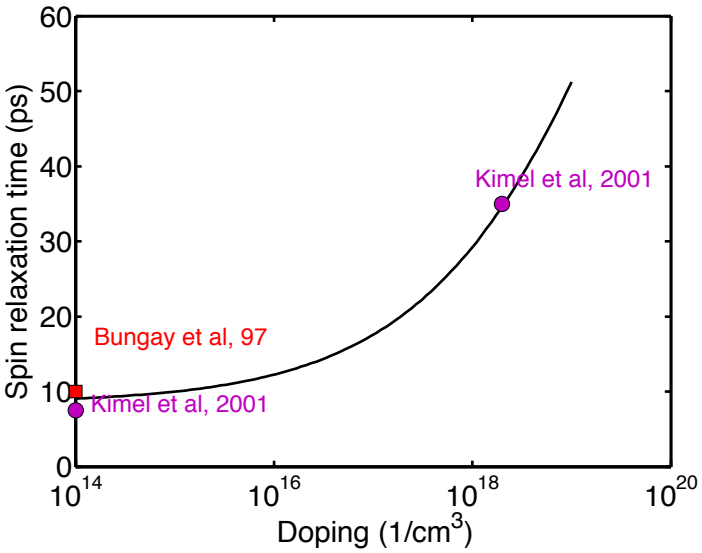

Figure 89: Spin relaxation time versus doping concentration in bulk GaAs at 300K. Experimental data points from Bungay & coworkers [27] and Kimel & coworkers [111] are also shown. The value of $Q\alpha^2$ is taken to be 0.012.

The spin-relaxation length is plotted as a function of T in Figure 90 for a doping concentration of 10^{16} cm^{-3}. The inset plot in Figure 90 shows that for non-degenerate doping levels in GaAs, the spin-relaxation length is independent of the doping concentration, and L_0 is approximately equal to 0.5 μm.

In the case of p-tye bulk GaAs, an additional spin-relaxation mechanism called the Bir-Aronov-Piks (BAP) must also be considered, especially at doping densities greater than 10^{18} cm^{-3} at 300K. According to the BAP mechanism, electron spin flip can occur due to the electron-hole scattering via exchange and annihilation interactions. However, in this research only n-type doping concentration is considered.

4.6 GaAs Quantum Wells

There is very little evidence that in GaAs quantum wells (QWs), mechanisms other than D'yakonov-Perel' might be relevant for spin relaxation. Both Dresselhaus bulk inversion asymmetry (BIA) and Bychkov-Rashba structural inversion asymmetry (SIA) must be accounted for to properly understand spin relaxation in QWs. Both

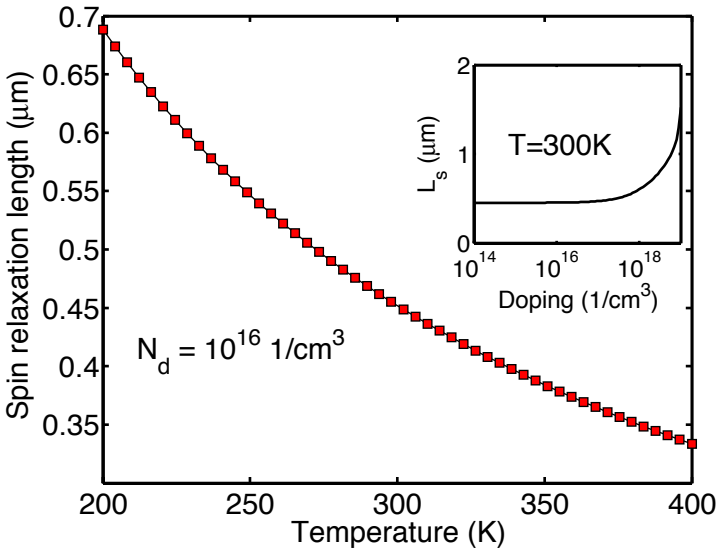

Figure 90: The temperature dependence of spin-relaxation length in bulk GaAs for non-degenerate doping levels. The inset plot shows the spin-relaxation length versus doping concentration in bulk GaAs at 300K.

BIA and SIA lead to spin splitting of the conduction band linear in $\mathbf{k}$, where $\mathbf{k}$ is the momentum vector.

The net spin-relaxation rate in GaAs quantum wells depends on the orientation of the quantum well. In addition, the spin-relaxation time also exhibits anisotropy. That is, the spin-relaxation rates parallel and perpendicular to the QW planes are different. Also, both BIA and SIA lead to different results for spin dephasing parallel and perpendicular to the QW planes. According to the Dresselhaus BIA, the spin-dephasing times for different crystal orientations of the QWs are listed in Table 25[4].

The factor τ_s^0 in equations given in Table 25 is given as

$$\frac{1}{\tau_s^0} = \frac{\alpha^2\hbar^2}{2m_c^2 E_g} E_k \tau_p \left(\frac{\pi}{W}\right)^2, \tag{146}$$

where W is the confining dimension of the quantum well, and m_c is the effective mass of the confined electrons.

[4]Check reference [61] for a complete description of the spin decoherence in QWs.

Table 25: Spin-relaxation time in GaAs QWs for various crystallographic orientations of the quantum well. Only the SOC due to bulk-inversion asymmetry is considered.

Crystal Orientation	Spin dephasing
[001]	$1/\tau_{s,\parallel} = 1/2\tau_{s,\perp} = 1/\tau_s^0$
[111]	$1/\tau_{s,\parallel} = 1/2\tau_{s,\perp} = 4/3\tau_s^0$
[110]	$1/\tau_{s,\parallel} = 1/4\tau_s^0$, $1/\tau_{s,\perp} = 0$

For the SIA, the spin-dephasing times are given as

$$\frac{1}{\tau_{s,\parallel}} = \frac{1}{2\tau_{s,\perp}} = \frac{1}{\tau_s^0}, \tag{147}$$

where τ_s^0 is given as

$$\frac{1}{\tau_s^0} = 4\alpha_{BR}^2 \frac{m_c}{\hbar^2} E_k \tau_p, \tag{148}$$

where α_{BR} is a parameter depending on the spin-orbit coupling and the asymmetry of the confining potential arising from the growth process of the heterostructure. α_{BR} can be tuned electrostatically, and this feature of α_{BR} is used for the conceptual idea of the Datta-Das spin FET. The interference of both BIA and SIA terms must be accounted for to evaluate the spin dephasing anisotropies in the quantum well. For a quantum well with the first quantized energy level, $E_{1e} \gg k_B T$, it can be shown using Eq. (146) that

$$\frac{1}{\tau_s} = Q\alpha^2 \tau_p \frac{E_{1e}^2}{\hbar^2} \frac{k_B T}{E_g}, \tag{149}$$

where Q depends on the dominant scattering mechanism in the quantum well. In 1996, Tackeuchi & coworkers [220] showed from their experiments that the relationship between τ_s and E_{1e} at room temperature for GaAs quantum wells is given as $\tau_s \propto E_{1e}^{-2.2}$. This is in good agreement with the DyP spin-relaxation mechanism for GaAs quantum wells as shown in Eq. (149) for the case when τ_p is independent of the well width. In 1999, Terauchi & coworkers [222] showed from their experiments that for their sample, $\tau_s \propto \mu^{-1}$, where μ is the measured hall mobility. This relationship

also confirms the presence of the DyP spin-relaxation mechanism in GaAs quantum wells. One of the most exhaustive experimental studies on the spin relaxation in GaAs QWs was conducted by Malinowski & coworkers in 2000 [137]. They showed that for bulk GaAs and for QWs with $E_{1e} < k_B T$ (wide quantum wells at high temperature) $\tau_s \propto T^3 \tau_p$. However, for QWs with $E_{1e} > k_B T$ (narrow wells at low temperature), $\tau_s \propto \tau_p T E_{1e}^2$. At high temperatures with dominant electron-phonon scatterings, τ_p for QWs and bulk GaAs is the same. Hence, for $T > 160K$, $\tau_s(QW)/\tau_s(BULK) \sim T^2$.

In general, $\tau_s \sim W^4/(T\tau_p(W,T)$. Hence, for the case when τ_p is independent of the well width, then τ_s varies as W^4, and τ_s also exhibits a linear increase with temperature. In Figure 91, the spin-relaxation time versus interconnect width is shown. The values of $Q\alpha^2$ chosen to match the theoretical models with experimental results lie between 3×10^{-4} to 9×10^{-4}. The product $Q\alpha^2$ determines the strength of the spin-orbit coupling leading to spin relaxation in the system. This value could be different for quantum wells and bulk materials [247].

The temperature-dependence of the experimentally-measured spin-relaxation time obtained for a 7.5 nm wide GaAs quantum well by Ohno & coworkers [166] is shown in Figure 92. Also shown in this figure is the spin-relaxation time obtained from our numerical simulations. There is a good match between the experimental and theoretical values of τ_s for the parameters selected in the simulation.

Using the numerical model of the spin-relaxation in GaAs QWs, the spin-relaxation length as a function of temperature is shown in Figure 93. The spin-relaxation length increases quadratically from 0.25 μm to 2.25 μm as the well width increases from 5 nm to 15 nm. It can be seen from the inset plot that the spin-relaxation length is nearly independent of temperature and is approximately 0.57 for all temperatures between 200K to 400K - a characteristic of the DyP mechanism.

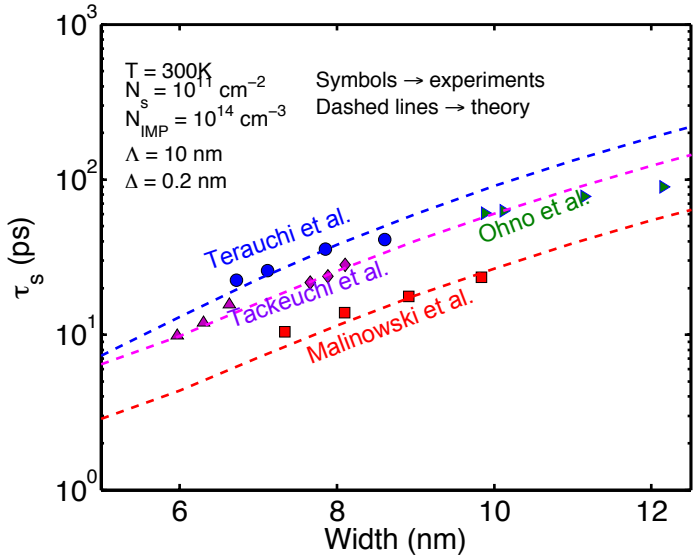

Figure 91: Spin-relaxation time in GaAs QWs versus the well width at 300K. Experimental data from Malinowski & coworkers [137], Terauchi & coworkers [222], Tackesuchi & coworkers [220], and Ohno & coworkers [166] are also shown. The simulation parameters chosen to provide best fit with experimental data points are given in the figure.

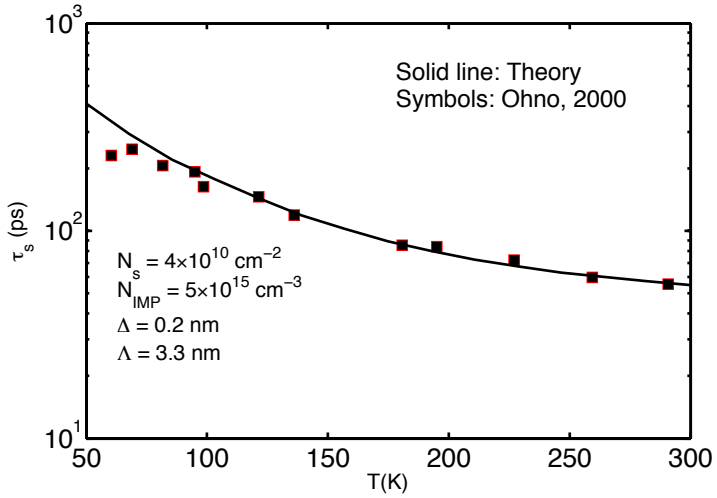

Figure 92: Spin-relaxation time versus the lattice temperature for a 7.5 nm wide GaAs QW. Also shown are the data points from experiments conducted by Ohno and coworkers [166].

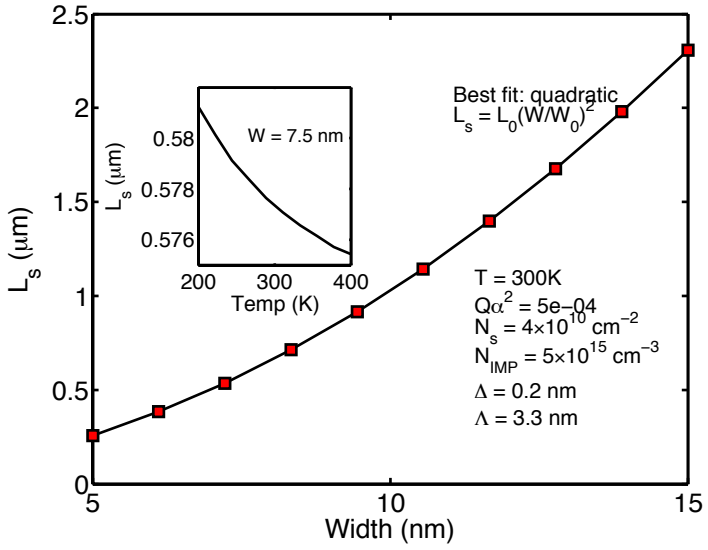

Figure 93: The spin-relaxation length in GaAs QW versus well width at 300K. The inset plot shows the temperature dependence of the spin-relaxation length in a 7.5 nm wide GaAs QW.

4.7 Conclusions

It is important that the information encoded in the electron spin variable be preserved over long distances. Otherwise, the rapid decay of the spin population in the interconnect will quickly restrict the signal span within the spin domain and will necessitate signal conversion into electrical domain or insertion of spin repeaters. In this chapter, physical models of spin-relaxation length of electrons in various materials in the presence of size effects are developed.

It is shown that in the case of metals and centrosymmetric semiconductor like Si, the dominant spin-relaxation mechanism is the Elliott-Yafet mechanism. According to this mechanism, the spin-relaxation time is directly proportional to the momentum-relaxation time. Since grain-boundary and sidewall scatterings tend to reduce the momentum-relaxation time, the spin-relaxation time is also adversely affected. In the case of metals, the spin-orbit coupling due to both defects and phonons are considered. To extract the values of spin-orbit couplings, experimental data on the spin-relaxation

length in metals at low and high temperatures are used. While the coupling at low temperatures is solely due to defects, the coupling at room temperature is primarily due to phonons. The best-case spin-relaxation length in Cu is 0.5 μm and that in Al is 0.62 μm at room temperature. It is found that for a 7.5 nm wide interconnect, the room temperature spin-relaxation length in Cu is 116 nm and that in Al is 165 nm, if the grain-boundary reflectivity is 0.2 and the sidewall specularity is zero.

The nature of spin relaxation in graphene changes from Elliott-Yafet to D'yakonov-Perel' type depending on the carrier concentration. For bulk graphene, the maximum achievable spin-relaxation length is ≈ 20 μm and occurs for carrier concentrations in excess of 10^{12} cm^{-2}. In the case of GNRs, the spin relaxation length for $W > 10$ nm is ≈ 17 μm for a curvature-induced spin-orbit coupling of 17 μeV. This value is little sensitive to the electron mean free path as the dominating spin-relaxation mechanism is the D'yakonov-Perel' one. There is a slight degradation in the spin-relaxation length with the interconnect widths in GNRs narrower than 5 nm.

In the case of the silicon, it is found that the spin-relaxation due to phonon-mediated SOC scales as T^{-3}, where T is the lattice temperature. The impurity-mediated SOC also leads to an Elliott-Yafet type of spin relaxation in Si. The room-temperature spin-relaxation length in Si for a doping level of 10^{18} cm^{-3} is found to be 1.4 μm. It is also discussed that the spin relaxation in silicon measured from non-local spin-valve techniques is more active due to the presence of contact contamination in the silicon channel.

Spin relaxation in both bulk and quantum wells of GaAs is governed by the DyP mechanism at high temperatures. The spin-relaxation length is, therefore, independent of the momentum-relaxation time in GaAs. It is found that for non-degenerately doped bulk GaAs, the spin-relaxation length at room temperature is 0.5 μm, and it scales as T^{-1} with temperature. In the case of GaAS QW, the room-temperature value of spin-relaxation length is found to depend on the electron concentration in

the well and the impurity concentration. At low background doping levels and low electron concentration ($\sim 10^{11}$ cm^{-2}), it is found that the R.T. spin-relaxation length is ≈ 0.57 μm; it is also shown that the spin-relaxation length is nearly independent of temperature.

The key findings of this chapter are summarized in Table 26, which lists the values of the spin-relaxation time and the spin-relaxation length in various materials studied in this research. Graphene offers the best-case spin-relaxation length at 300K, while copper has the shortest spin-relaxation length amongst all the materials studied.

Table 26: Spin-relaxation time and spin-relaxation length at 300K in various materials. The interconnect width is 7.5 nm unless otherwise mentioned. For graphene, the effective SOC is approximated by the ripple-induced SOC of 17 μeV. N_d is the n-type doping concentration in the semiconductor, N_s is the electron concentration in the quantum well, and N_{IMP} is the background doping concentration in the quantum well.

Material	τ_s (ps)	L_s (μm)
Copper (R = 0.145, p = 0)	2.59	0.07
Aluminum (R = 0.5, p = 0)	4.52	0.1
Graphene nanoribbons (E_f = 0.2 eV, P_{GNR} = 0.2)	2.28×10^4	17
Silicon ($N_d = 10^{18}$ cm^{-3})	1660	1.4
GaAs (bulk) ($N_d = 10^{17}$ cm^{-3})	17.6	0.47
GaAs (QW) ($N_s = 10^{11}$ cm^{-2}, $N_{IMP} = 10^{14}$ cm^{-3})	33	0.57

CHAPTER V

SPIN INJECTION AND TRANSPORT IN ALL-SPIN LOGIC

Logic devices based on electron-spin state variable fall broadly into two categories of devices [161] - (i) devices in which the input and the output are in electrical domain while the processing within the device uses the electron spin as an auxiliary to the electron charge and (ii) devices in which the input and the output are also in the spin domain [161]. Examples of the devices that fall into the former category include the spin-FET [212], the magnetic-tunnel-junction (MTJ) logic [249], the all-spin-logic (ASL) device [14], and the Datta-Das spin modulator [42]. The devices that belong to the latter category include the spin wave bus (SWB) devices [109], magnetic-domain-wall majority gates [2], and the magnetic cellular automata (MQCA) [89]. However, the latter category of devices require an Amperian magnetic field to communicate information. Scaling down the footprints of these devices is challenging because the requirement on critical magnetic field for computation increases with scaling [7]. However, in the case of an ASL device, the requirement on critical electric current to switch the magnetization of nanomagnetic devices reduces with technology scaling. Hence, the switching of nanomagnets with pure spin currents is quite amenable to dimensional scaling.

In this chapter, the ASL device is used as the prototype of a switching element in the spin domain. The following analyses are conducted in this chapter for the ASL device. First, the standard model of spin injection as developed by Valet and Fert and also outlined in [253] is applied to the lateral non-local spin-valve geometry of the ASL device to obtain the steady-state profile of spin currents in the ASL device.

Second, the impact of (i) material properties of the channel, (ii) the interconnect length between the transmitter and the receiver nanomagnets, and (iii) the size effects is investigated on the efficiency of spin injection and transport in the ASL device. The chapter is concluded by summarizing the important findings.

5.1 Spin injection and transport efficiency

A lateral non-local spin valve is shown in Figure 14 of Chapter II. This structure forms the heart of the ASL device proposed by Datta & coworkers [14]. Another variant of the ASL device is shown in Figure 94, where the second contact in the transmitter is placed at the bottom of the interconnect so that the electrical-current path can be completely separated from the spin-current path. In the ASL device, a non-equilibrium population of electron spins (also called "spin accumulation") can be created in the non-magnetic interconnect by making an electric current flow in the transmitter of the ASL device.

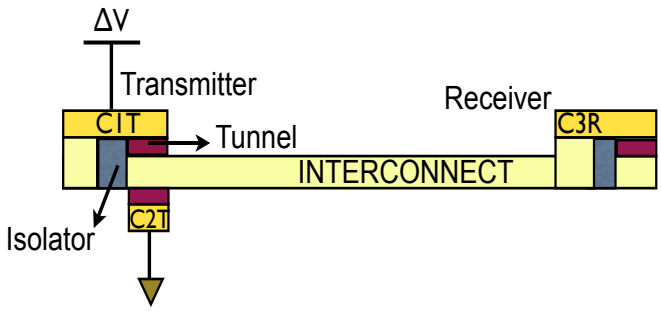

Figure 94: An ASL device, where CIT and C2T form the transmitter electrodes and C3R is the receiver electrode. C1T and C3R are magnetic, while C2T is non-magnetic.

In the case of a ferromagnet, there is a difference in the density of states of majority and minority electron spins at the Fermi level (see Figure 95). This difference in the density of states transcends to a difference in the relaxation time, mean free path, mobility, diffusivity, and conductivity of up-spin and down-spin electrons/carriers for the ferromagnet.

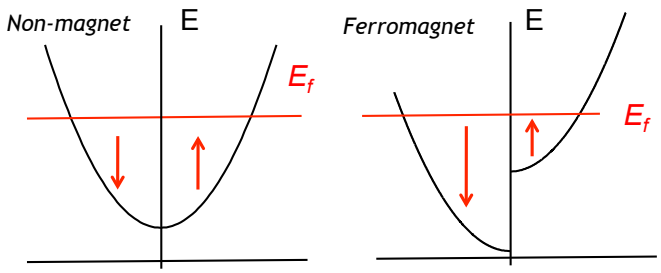

Figure 95: The left figure shows that the density of states at the Fermi level is equal for both spin-up and spin-down carriers for a non-magnet. The right figure shows that the density of states for the up-spin and down-spin carriers is different at the Fermi level for a ferromagnet.

The electrical current, j, and the spin current, j_s, in any material are given by the following coupled equations:

$$j = j_\uparrow + j_\downarrow = \sigma\nabla\mu + \sigma_s\nabla\mu_s, \tag{150a}$$

$$j_s = j_\uparrow - j_\downarrow = \sigma_s\nabla\mu + \sigma\nabla\mu_s, \tag{150b}$$

where $\sigma = \sigma_\uparrow + \sigma_\downarrow$ is the net electrical conductivity of the system, $\sigma_s = \sigma_\uparrow - \sigma_\downarrow$ is the spin conductivity of the system, $\nabla\mu = 1/2\nabla(\mu_\uparrow + \mu_\downarrow)$ is the gradient in the quasi-chemical potential, and $\nabla\mu_s = 1/2\nabla(\mu_\uparrow - \mu_\downarrow)$ is the gradient in the spin quasi-chemical potential. In the case of a ferromagnet, a non-equilibrium spin gradient creates a charge current, while an applied bias can create a spin current. In normal non-magnetic conductors, due to the absence of σ_s, only an applied bias is insufficient to create a spin-polarized current. However, if $\nabla\mu_s$ is created in the non-magnetic material by interfacing it with a ferromagnetic material and applying a bias to the structure, a spin-polarized current can be made to flow through the non-magnetic material. The spin-polarized current through a material can also be expressed as

$$j_s = P_\sigma j + 4\frac{\sigma_\uparrow\sigma_\downarrow}{\sigma}\nabla\mu_s, \tag{151}$$

where P_σ is the conductivity polarization of the material and is given as

$$P_\sigma = \frac{\sigma_\uparrow - \sigma_\downarrow}{\sigma_\uparrow + \sigma_\downarrow}. \tag{152}$$

In a degenerate conductor, the spin quasi-chemical potential, μ_s, follows a diffusion equation that is given as

$$\nabla^2 \mu_s = \frac{\mu_s}{L_s^2}, \tag{153}$$

where L_s is the spin-relaxation length and is given as

$$L_s = \sqrt{\overline{D}\tau_s}, \tag{154}$$

where $\overline{D}$ is the spin-averaged diffusion coefficient of carriers in the system and is mathematically expressed as

$$\overline{D} = \frac{(N_\uparrow + N_\downarrow)\, D_\uparrow D_\downarrow}{N_\uparrow D_\uparrow + N_\downarrow D_\downarrow}, \tag{155}$$

where $N_\uparrow(D_\uparrow)$ and $N_\downarrow(D_\downarrow)$ are the density of states (diffusivity) corresponding to up-spin and down-spin carriers, respectively.

Clearly, the fundamental issues applicable to an ASL device are identifiable from its representation in Figure 94. These issues are: (i) efficient injection of electron spins into the device, (ii) low-loss transport of electron spins between the devices, and (iii) efficient detection of spins at the receiver. These fundamental issues of the ASL device can be quantified through a figure of merit called the spin injection & transport efficiency (SITE). The SITE in the ASL device gives the amount of the spin current per unit input electrical current reaching the receiver at $x = L$, where L is the interconnect length. In this sense, SITE incorporates the losses encountered in spin signal (i) upon injection from the ferromagnet into the interconnect captured through "spin-injection efficiency (SIE)" parameter, and (ii) in transportation through the interconnect, which is captured through the parameter "transport efficiency (TE)". Mathematically,

$$SITE = SIE \times TE. \tag{156}$$

Once the fundamental issues in implementing ASL are overcome, circuit- and architecture-level issues will need to be addressed. These issues are related to achieving a high

performance while maintaining a low power consumption for the spin logic and will be discussed in Chapter VI.

To evaluate SITE in the ASL device, the spin quasi-chemical potential equation (Eq. (153)) is solved in each region of the structure and appropriate boundary conditions are applied. In the presence of a tunnel barrier at the interface between the ferromagnetic electrodes and the interconnect, there is a discontinuity in the spin quasi-chemical potential, which is captured through the conductance of the interface and its spin selectivity. The polarization j_s/j of the current flowing through the interface is given as

$$P_{j,int} = \left(\frac{j_s}{j}\right)_{int} = P_\Sigma + \frac{\Sigma'_{int}}{j}\Delta\mu_{s,int}, \tag{157}$$

where P_Σ is the conductance polarization of the interface (also called the spin selectivity), $\Delta\mu_{s,int}$ is the discontinuity in the spin quasi-chemical potential at the interface, and Σ'_{int} is given as

$$\Sigma'_{int} = 4\frac{\Sigma_\uparrow\Sigma_\downarrow}{\Sigma_{int}}. \tag{158}$$

The interface resistance for various combinations of magnetic/non-magnetic layers has been computed using first-principles model calculations [210], [193]. The calculation of the interface resistance takes into account the disorder, surface roughness, and different scattering mechanisms [253]. However, in the following analysis, we consider that an additional oxide barrier with a high spin selectivity such as MgO or Al_2O_3 has been introduced between the ferromagnet and the interconnect[1]. The electrical resistance area product (ERAP) and the spin selectivity of the tunnel barrier are parametrized.

[1]It must be noted that in the ASL proposal by Datta et al., there are no tunnel barriers for metallic channels. However, in our implementation we retain tunnel barriers because unlike devices, interconnects will typically be longer than the spin-relaxation length causing a rapid degradation in SITE with an interconnect length for an ASL device without tunnel barriers.

The mathematical formalism to evaluate the SITE in the ASL device is described below.

5.1.1 Mathematical formalism

The cross-sectional view of the ASL device with the direction of flow of electron spins is depicted in Figure 96.

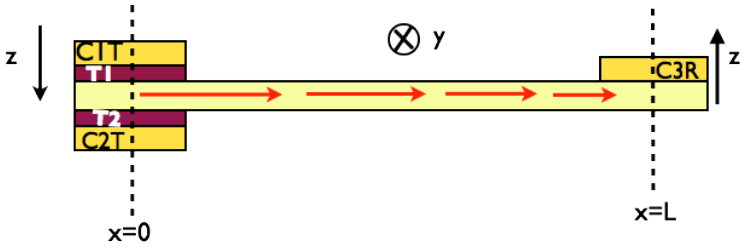

Figure 96: The cross-sectional view of the ASL device. The arrows in the interconnect show the flow of electron spins.

Even though the problem of evaluating the efficiency of spin injection and transport in the ASL device is a two-dimensional problem, the problem can be decoupled into two one-dimensional problems. If it is assumed that the contact dimensions and the thickness of the non-magnetic region are much smaller than the spin-diffusion length of electrons in the non-magnetic region, then the spin diffusion in the non-magnetic conductor can be considered as one dimensional.

Using Eqs. (151) and (153), the spin quasi-chemical potential and the spin current in the various regions of the ASL device are given below.

Ferromagnetic transmitter terminal C1T

$$\mu_{SC1}(z) = a_1 e^{z/L_{SF}} + a_2 e^{-z/L_{SF}}. \tag{159a}$$

$$j_{SC1} = P_{\sigma C1} j + 4\frac{\sigma_{1\uparrow}\sigma_{1\downarrow}}{\sigma_1 L_{SF}}\left(a_1 e^{z/L_{SF}} - a_2 e^{-z/L_{SF}}\right). \tag{159b}$$

Tunnel T1

$$j_{ST1} = P_{\Sigma 1} j + 4\frac{\Sigma_{1\uparrow}\Sigma_{1\downarrow}}{\Sigma_1}\Delta\mu_s^{int}. \tag{160}$$

Non-magnet $0 \leq z \leq t_{INT}$

$$\mu_{SN}(z) = be^{z/L_{SN}} + ce^{-z/L_{SN}}. \tag{161a}$$

$$j_{SN}(z) = \frac{\sigma_N}{L_{SN}} \left(be^{z/L_{SN}} - ce^{-z/L_{SN}} \right). \tag{161b}$$

Tunnel T2

$$j_{ST2} = \Sigma_2 \left(d_1 e^{t_{INT}/L_{SN2}} + d_2 e^{-t_{INT}/L_{SN2}} - be^{t_{INT}/L_{SN}} - ce^{-t_{INT}/L_{SN}} \right). \tag{162}$$

Non-magnetic transmitter terminal C2T

$$\mu_{SC2}(z) = d_1 e^{z/L_{SN2}} + d_2 e^{-z/L_{SN2}}. \tag{163a}$$

$$j_{SC2} = \frac{\sigma_{N2}}{L_{SN2}} \left(d_1 e^{z/L_{SN2}} - d_2 e^{-z/L_{SN2}} \right). \tag{163b}$$

Non-magnetic interconnect $0 \leq x \leq L$

$$\mu_{SN}(x) = fe^{x/L_{SN}} + ge^{-x/L_{SN}}. \tag{164a}$$

$$j_{SN}(x) = \frac{\sigma_N}{L_{SN}} \left(fe^{x/L_{SN}} - ge^{-x/L_{SN}} \right). \tag{164b}$$

Ferromagnetic receiver terminal C3R

$$\mu_{SC3}(z) = h_1 e^{z/L_{SF}} + h_2 e^{-z/L_{SF}}. \tag{165a}$$

$$j_{SC3} = 4\frac{\sigma_{3\uparrow}\sigma_{3\downarrow}}{\sigma_3 L_{SF}} \left(h_1 e^{z/L_{SF}} - h_2 e^{-z/L_{SF}} \right). \tag{165b}$$

The spin current at each interface is balanced, and the spin accumulation at the boundary of the system (defined by ferromagnets) is assumed to be zero. These conditions are mathematically given as the set of following ten equations.

$$a_1 e^{-t_{C1}/L_{SF}} + a_2 e^{t_{C1}/L_{SF}} = 0. \tag{166a}$$

$$d_1 e^{(t_{INT}+t_{C2})/L_{SN2}} + d_2 e^{-(t_{INT})+t_{C2}/L_{SN2}} = 0. \tag{166b}$$

$$b + c = f + g. \tag{166c}$$

$$f e^{L/L_{SN}} + g e^{-L/L_{SN}} = 0. \tag{166d}$$

$$h_1 e^{t_{C3}/L_{SF}} + h_2 e^{-t_{C3}/L_{SF}} = 0. \tag{166e}$$

$$P_{\sigma C1} j + 4\frac{\sigma_{1\uparrow}\sigma_{1\downarrow}}{\sigma_1 L_{SF}}(a_1 - a_2) = P_{\Sigma 1} j + 4\frac{\Sigma_{1\uparrow}\Sigma_{1\downarrow}}{\Sigma_1}(b + c - a_1 - a_2). \tag{166f}$$

$$P_{\Sigma 1} j + 4\frac{\Sigma_{1\uparrow}\Sigma_{1\downarrow}}{\Sigma_1}(b + c - a_1 - a_2) = \frac{\sigma_N}{L_{SN}}(b - c) + \frac{\sigma_N}{L_{SN}}(f - g). \tag{166g}$$

$$\frac{\sigma_N}{L_{SN}}\left(b e^{t_{INT}/L_{SN}} - c e^{-t_{INT}/L_{SN}}\right) = \Sigma_2\left(d_1 e^{t_{INT}/L_{SN2}} + d_2 e^{-t_{INT}/L_{SN2}} - b e^{t_{INT}/L_{SN}} - c e^{-t_{INT}/L_{SN}}\right). \tag{166h}$$

$$\frac{\sigma_N}{L_{SN}}\left(b e^{t_{INT}/L_{SN}} - c e^{-t_{INT}/L_{SN}}\right) = \frac{\sigma_{N2}}{L_{SN2}}\left(d_1 e^{t_{INT}/L_{SN2}} - d_2 e^{-t_{INT}/L_{SN2}}\right). \tag{166i}$$

$$\frac{\sigma_N}{L_{SN}}\left(f e^{L/L_{SN}} - g e^{-L/L_{SN}}\right) = 4\frac{\sigma_{3\uparrow}\sigma_{3\downarrow}}{\sigma_3 L_{SF}}(h_1 - h_2). \tag{166j}$$

The first five equations in the above set of equations correspond to balancing spin quasi-chemical potential at the interfaces, while the last five equations correspond to balancing spin currents at the interfaces[2]. From the above formalism, the various efficiency parameters are given as

$$SIE = \frac{\sigma_N}{L_{SN}}\frac{f - g}{j}, \tag{167a}$$

$$TE = \frac{f e^{L/L_{SN}} - g e^{-L/L_{SN}}}{f - g}, \tag{167b}$$

$$SITE = SIE \times TE = \frac{\sigma_N}{L_{SN}}\frac{f e^{L/L_{SN}} - g e^{-L/L_{SN}}}{j}. \tag{167c}$$

The SITE of an ASL device depends upon two factors: relative spin resistance-area products (SRAPs)[3] of the injecting ferromagnet, the tunnel barrier, and the interconnect and (ii) the length of the interconnect relative to the spin-relaxation length. As the resistivity of the interconnect material increases or its length increases relative to the spin-relaxation length, the SITE of the ASL device degrades. In the next two subsections, the impact of the interface resistance and the interconnect length on the various efficiencies for the ASL device is analyzed.

[2]The spin current balance equations will need to be modified if the cross-sectional dimensions for the spin current flow in the z- and the x-directions are different.

[3]SRAP is defined as the product of the resistivity and the spin-relaxation length in the case of a non-magnetic conductor. For ferromagnets, SRAP is equal to the ratio of the product ($\rho \times L_{SF}$) and ($1\text{-}P_\sigma^2$).

5.1.2 Impact of interface resistance on spin injection and transport

In Figure 97, SIE and TE are both plotted as a function of the interface ERAP for various values of the conductivity polarization of the injecting ferromagnet. The interconnect length has been fixed to 1 μm. It is also assumed that the cross-sectional areas of various elements in the ASL geometry can be factored out. As seen from this figure, an increase in ERAP and/or P_σ(FM) improves SIE. However, TE is insensitive to the interface properties and depends only on the interconnect length. Further, SIE saturates to the conductivity polarization of the injecting ferromagnet when ERAP of the interface is sufficiently high such that the interface acts like a tunnel barrier.

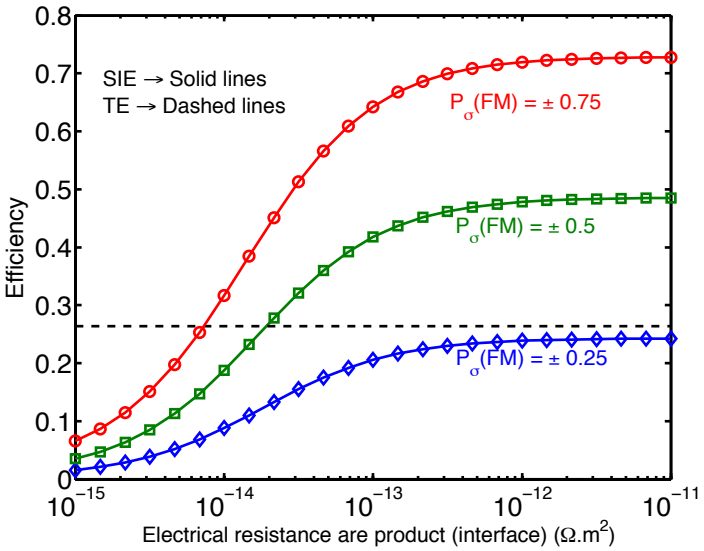

Figure 97: Spin injection efficiency versus electrical resistance area product (ERAP) of the interface between the ferromagnet and the interconnect. The horizontal dashed line is the transport efficiency which is independent of the interface properties and depends only on the interconnect length. Material parameter values are: ρ(FM) = 7.8×10^{-9} Ω.m, ρ(NM) = 2×10^{-8} Ω.m, t_{INT} = 15 nm, $t_{C1} = t_{C2} = t_{C3}$ = 10 nm, L_{SF} = 10 nm, $L_{SN} = L_{SN2}$ = 0.5 μm.

In Figure 98, the SITE of the ASL device as a function of the ERAP of the interface is shown. The nature of SITE versus ERAP of the interface is the same as that of SIE versus the interface ERAP. This is because SITE is given as the product of SIE

and TE, and it is only SIE that depends on the interface characteristics, while TE is independent of the interface characteristics. Hence, SITE improves as the ERAP of the interface increases. For an interconnect length $L << L_{SN}$, the transport efficiency will tend toward unity; therefore, SITE will saturate to the conductivity polarization of the injecting ferromagnet, $P_{\sigma C1}$. It can also be seen from this figure that the value of SITE increases with an increase in the conductivity polarization of the ferromagnet.

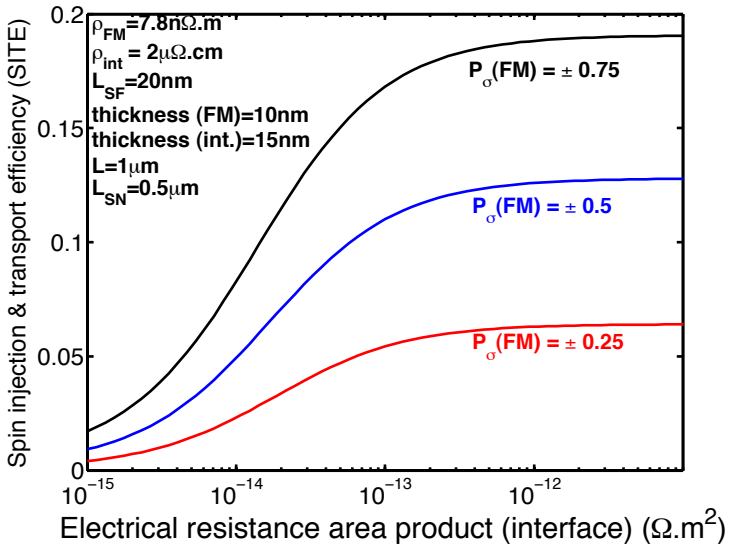

Figure 98: Spin injection and transport efficiency versus the electrical resistance-area-product of the tunnel barrier.

For a half-metal ferromagnet in which $P_\sigma \rightarrow 1$, the SITE of the ASL would also tend to unity without the need of a large interface resistance. Half metals are magnetically oriented compounds for which the electrons of one spin orientation have metal-like energy bands, whereas electrons of the opposite spin encounter an energy gap about the Fermi energy. Since half metals, by definition, have electrons of only one spin state present at the Fermi energy, they are potential candidates for use as high efficiency spin injectors. Examples include half metallic oxides such as CrO_2, Fe_3O_4, Heusler alloys, and double pervoskites. For typical elemental ferromagnets

such as Fe, Co and Ni, the spin-conductivity polarization is 40%, 34%, and 23% respectively [52]. In contrast to the half metals, elemental ferromagnets order well above room temperature, and their properties from a physics and materials point-of-view are well understood.

5.1.3 Impact of interconnect length on spin injection and transport efficiency

In Figure 99, the efficiencies of spin injection and spin transport for the ASL circuit are plotted as a function of the interconnect length. While the value of SIE is independent of the interconnect length, the value of TE degrades exponentially with interconnect length. However, an improvement in the spin-relaxation length, L_{SN}, in the interconnect material can significantly improve the value of SITE.

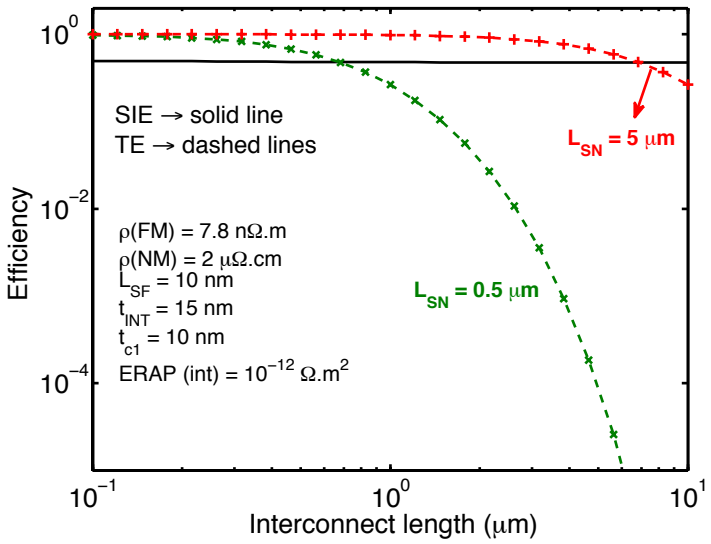

Figure 99: Efficiencies of spin injection (SIE) and transport (TE) versus interconnect length for an ASL device. Material parameter values used in the simulation are given in the figure.

Using the results of SIE and TE, the SITE of the ASL device is shown in Figure 100 as a function of the interconnect length. The SITE degrades rapidly with an increase in the interconnect length. As seen from this figure, the value of SITE drops from by

three orders of magnitude as the interconnect length increases from 1 μm to 10 μm for L_{SN} = 0.5 μm. A degradation in SITE either due to conductivity mismatch or long length of the interconnect could lead to an incorrect signal detection at the receiver electrode, particularly if the receiver is less sensitive. This fundamental limitation of an ASL circuit can be addressed by (i) increasing the input electrical current in the transmitter at the cost of Joule heating, (ii) reducing the nanomagnet size to improve its sensitivity at the cost of its reduced thermal stability, (iii) inserting spin repeaters along the interconnect to compensate for signal losses at the cost of circuit area, and (iv) designing smart spin architectures that favor short-distance communication.

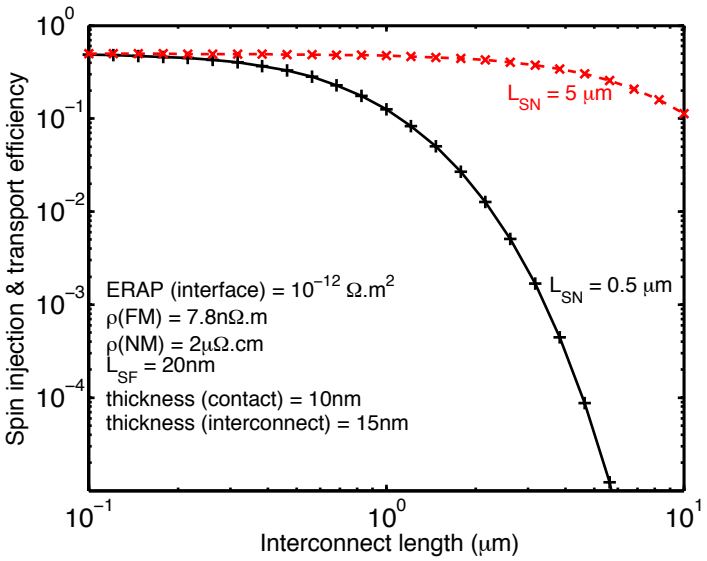

Figure 100: SITE versus interconnect length. The material and design parameters used for the simulation are given in the figure.

In the next sections, the impact of using different interconnect materials and dimensional scaling only on the SITE of the ASL device is quantified, because SITE captures the net signal losses within the ASL device. The impact of varying the cross-sectional area in the 2D geometry of the ASL device has been incorporated in the simulation framework. Unless otherwise specified, the ferromagnet injectors and detectors and the tunnel barriers have a cross-sectional dimension of 130 nm^2,

considering them to be an elliptical body with major- and minor-axis dimensions of 16.5 nm and 10 nm, respectively. The aspect ratio in case of metallic (Cu & Al) and semiconducting (Si & GaAs) interconnects is taken to be two. For single-layer GNR interconnects, the thickness is taken to be 0.35 nm.

5.2 Interconnects for Spin Logic

The SITE of an ASL device with various interconnect materials is evaluated. While metallic interconnects have a lower electrical resistivity that reduces the problem of "conductivity mismatch" in spin circuits, their spin-relaxation length can be shorter than few 100's of nm that can limit the maximum obtainable SITE for a given interconnect length. Graphene nanoribbons have a long spin-relaxation length; however, the presence of quantum resistance even for ultra short interconnects could limit the SITE of the ASL device with GNR interconnects. Addition of multiple layers within the GNR stack may help to improve SITE only when the layers are coupled to each other. In the case of only a weak coupling between the parallel layers, the best-case SITE obtained in an ML-GNR stack will be limited. The electrical and spintronic properties of semiconducting interconnects can be tuned through the doping concentration. However, their resistivity is still much higher than that of ferromagnets necessitating the insertion of highly resistive spin-selective oxide barriers in the ASL device to be able to achieve an appreciable SITE.

5.2.1 Metallic interconnect in the all-spin logic

Metals like Cu and Al may serve as the non-magnetic interconnect to carry spin currents in the ASL device to establish communication between ferromagnetic drivers and receivers. Due to dimensional scaling and size effects, the spin-relaxation length in metals is adversely affected as discussed in Chapter IV. The limited spin-relaxation lengths in metals can easily put an upper bound on the spacing between the transmitter and the receiver for a given threshold spin current of the receiver ferromagnet.

Figure 101 shows the SITE of the ASL device with metallic interconnects versus the interconnect width. In the absence of any size effects, the SITE is independent of the interconnect width. For Al interconnects in the ASL, the best-case SITE is 0.18, while for Cu interconnects, the best-case SITE is 0.13 for a 1 μm long interconnect. At the same interconnect length, the SITE of the ASL with Cu interconnects drops to 1.52×10^{-4} (point "a" in Figure 101) and that in Al drops to 2×10^{-3} (point "b" in Figure 101) for a 7.5 nm wide interconnect having a grain-boundary reflectivity, $R = 0.2$, and a sidewall specularity, $p = 0$. Such low values of SITE result from a degradation in the spin-relaxation length of metallic conductors in the presence of size effects at narrow dimensions.

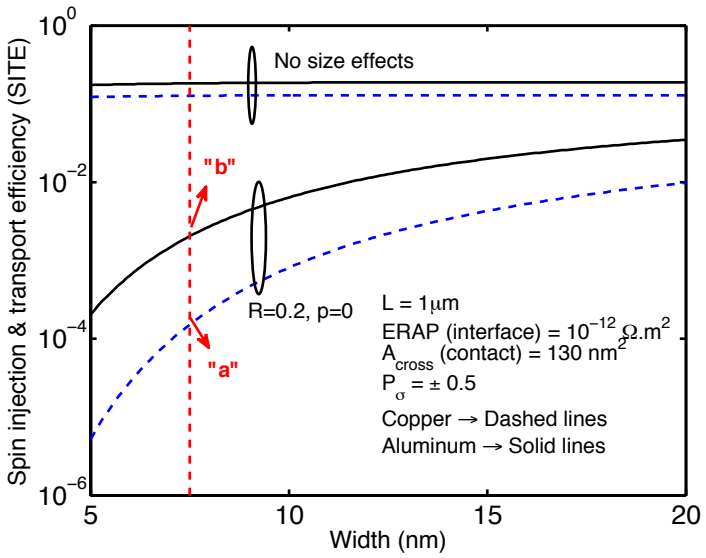

Figure 101: Spin injection and transport efficiency in an ASL circuit versus the interconnect width. The aspect ratio of the interconnect is assumed to be two. The material properties of the ferromagnet are the same as provided in Figure 99. Points "a" and "b" show the value of SITE at 7.5 nm width.

The impact of grain-boundary reflectivity and sidewall specularity on the SITE of an ASL device with a 7.5 nm wide metallic interconnect is shown in Figure 102. For a change in R from 0.1 to 0.5, the SITE degrades by four orders of magnitude for L = 1 μm and p = 0. The SITE of an ASL device with metallic interconnects

decreases with a decrease in the sidewall specularity. The presence of size effects can vastly degrade the amount of spin current available at the receiver terminal in the ASL circuit.

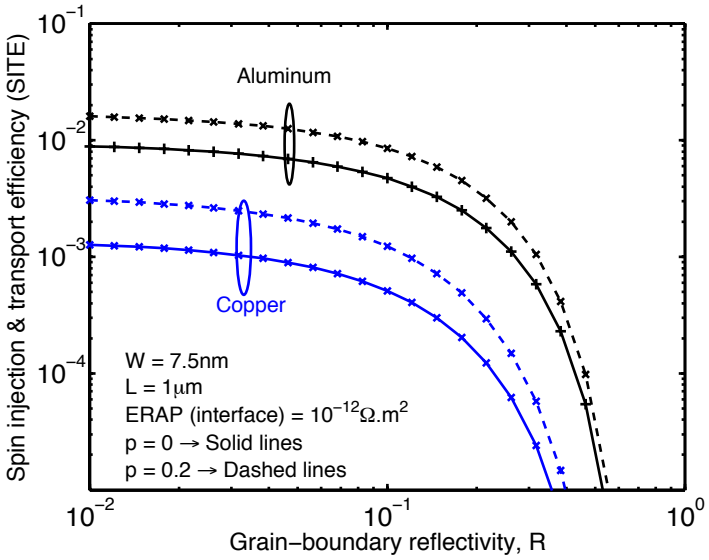

Figure 102: The impact of size effect parameters on the SITE of an ASL device with metallic interconnects. The interconnect width and length are 7.5 nm and 1 μm, respectively.

5.2.2 Graphene nanoribbons in the all-spin logic

In the case of graphene nanoribbons, the tunnel barriers are fabricated on the top of the graphene sheet. To evaluate SITE in spin valves with graphene nanoribbon interconnects, the contact resistance according to Landauer's formula is given as

$$R_{int} = \frac{h}{4e^2}\frac{1}{N_{ch}T}, \tag{168}$$

where $h/4e^2$ is identified as one-half of the quantum resistance ($= Rq/2$), N_{ch} is the number of conduction channels, and T is the transmission probability of electrons from the contact into the graphene channel. If the interface between the magnetic contact and the graphene channel does not introduce any mixing of electron spins,

then the net resistance for up-spin and down-spin carriers can be computed as

$$R_{CT\uparrow} = \frac{h}{e^2}\frac{1}{N_{ch}T_{\uparrow}}, \tag{169a}$$

$$R_{CT\downarrow} = \frac{h}{e^2}\frac{1}{N_{ch}T_{\downarrow}}, \tag{169b}$$

where $T_{\uparrow}$ and $T_{\downarrow}$ are the transmission coefficients for up-spin and down-spin carriers, respectively. These transmission coefficients are related to the net transmission coefficient, T, for electrons, and the spin polarization, P_{Σ}, of the transmission coefficient. That is,

$$T_{\uparrow} = (1 + P_{\Sigma})\frac{T}{2}, \tag{170a}$$

$$T_{\downarrow} = (1 - P_{\Sigma})\frac{T}{2}. \tag{170b}$$

For highly-resistive tunnel barriers that are employed at the transmitter side to overcome the conductivity mismatch, the net transmission coefficient, T_{TX} is generally very low. However, the receiver side does not have any tunnel barriers, which makes the receiver-side transmission coefficient $T_{RX} > T_{TX}$. In this analysis, T_{RX} is selected to be 0.5, unless otherwise stated. The spin polarization of the transmission coefficient, P_{Σ}, is optimistically selected to be ± 0.5 for simulations. Only one of the contacts in the transmitter side is assumed to be ferromagnetic in nature, while the other contact is a normal metal. Further, the polarity of the receiver magnetization is assumed to be opposite to that of the transmitter electrode.

In Figure 103, the spin injection and transport efficiency in the ASL circuit with GNR interconnects is plotted as a function of the GNR width. Some very important conclusions can be drawn from the simulation results of Figure 103. SITE degrades rapidly with an increase in interconnect length, an increase in the edge-scattering coefficient, and a decrease in the interconnect width particularly for non-zero P_{GNR}. SITE degrades by a factor of $5\times$ as the interconnect length increases from 1 μm to 10 μm for an edge-scattering coefficient of zero for wider ribbons. For $P_{GNR} = 0.2$,

the SITE degrades rapidly as the interconnect width decreases. For example, at an interconnect length of 1 μm, SITE degrades from 0.2 to 0.1 as the interconnect width scales from 20 nm to 5 nm.

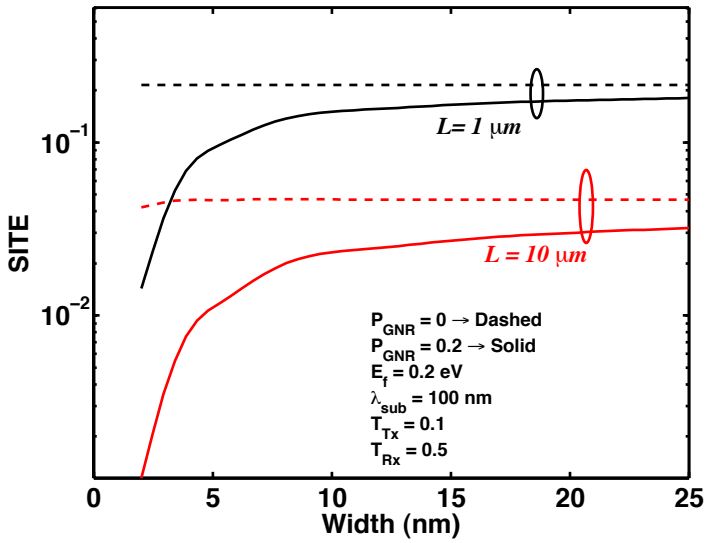

Figure 103: Spin injection and transport efficiency versus interconnect width in GNR. The substrate-limited MFP is taken to be 100 nm, which is a characteristic value for SiO_2 substrates. Here L is the interconnect length.

With ML-GNR, the SITE would increase with an increase in the number of layers only when the c-axis resistivity is comparable to that of HOPG as shown in Figure 104. With $\rho_m = 100\rho_m(\text{HOPG})$, the value of SITE saturates to 0.175 and addition of more layers does not help to improve SITE. This scenario is changed when $\rho_m = \rho_m(\text{HOPG})$ when the value of SITE increases from 0.13 to 0.28 as the number of layers increases from unity to 10 for a 7.5 nm wide GNR with $P_{GNR} = 0.2$ and $E_f = 0.2$ eV.

As mentioned in Chapter IV, the spin-relaxation length in wide graphene flakes is found to lie between (1-2) μm in most experiments. Hence, it is important to know the impact of spin-relaxation length on SITE. In Figure 105, the SITE of the ASL circuit is plotted as a function of L_s varying from 100 nm to 10 μm for a 7.5

nm wide GNR with an edge roughness of 20% and E_f = 0.2 eV. It can be seen from the figure that the when $L/L_{SN} >> 1$, the SITE degrades rapidly with a reduction in L_{SN}. Such a degradation in SITE requires an enormous increase in the input electrical current at the transmitter to overcome the losses in the spin current encountered in the interconnect. This would translate to a rapid increase in the energy dissipation of the spin interconnect. Further, SITE increases with a decrease in the net transmission coefficient of the transmitter. This is because a low value of T_{TX} improves the spin filtering at the interface by minimizing the conductivity mismatch between the ferromagnet and the interconnect. This difference in SITE for different T_{TX} is more apparent when the losses in the interconnect are reduced. That is, when $L/L_{SN} < 1$, then the improvement in SITE with a lower T_{TX} is more evident.

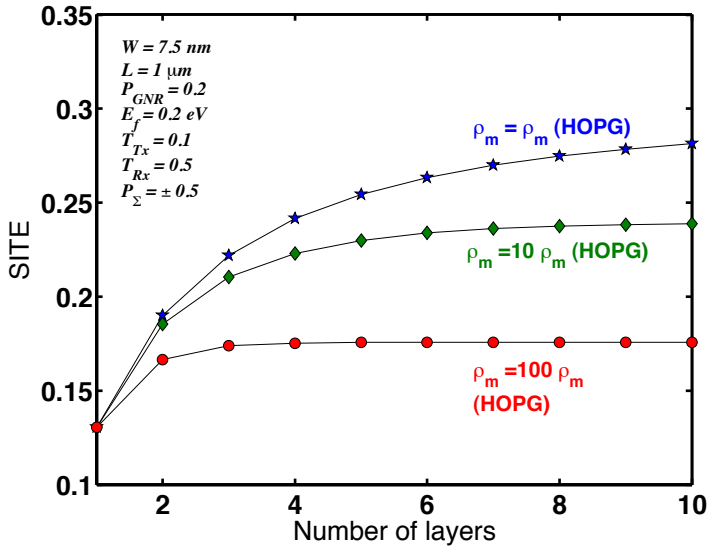

Figure 104: Spin injection and transport efficiency versus the number of layers in ML-GNR for a 1 μm long and 7.5 nm wide interconnect.

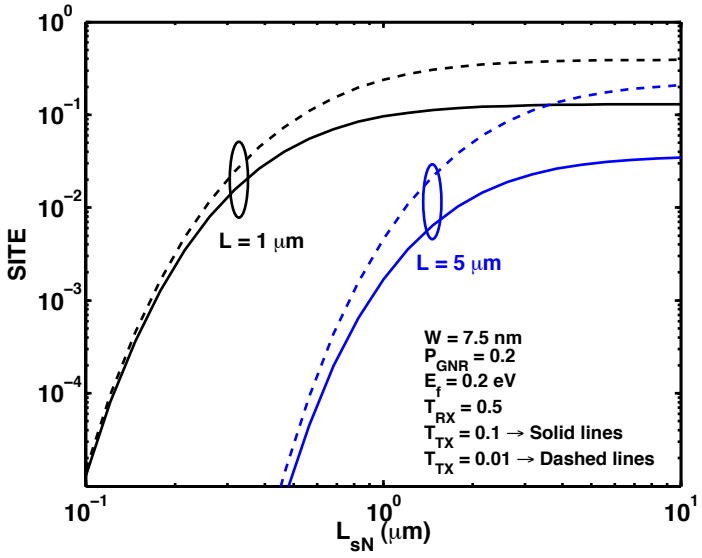

Figure 105: Spin injection and transport efficiency versus spin-relaxation length in a 7.5 nm wide GNR.

5.2.3 Semiconducting interconnects in the all-spin logic

The SITE of the ASL device with semiconducting interconnects can be changed by changing the doping concentration. This is because both the semiconductor resistivity and its spin-relaxation length are a function of the doping concentration. In the case of silicon, as the doping increases, the spin-relaxation length and the resistivity reduce. This lowers the SRAP of silicon, which can help to improve the SITE. However, a reduction in the spin-relaxation length also increases the signal loss within the interconnect. Hence, an optimal doping concentration can be determined that maximizes the SITE of the ASL device with a silicon interconnect. In Figure 106, the SITE of the ASL device with Si interconnect is shown as a function of doping concentration for various lengths of the interconnect. The ERAP of the interface is assumed to be $10^{-9}\ \Omega.m^2$. For this simulation, low-bias, flat-band condition is assumed in the semiconductor. It can be seen from Figure 106 that there is an optimal doping concentration for which the SITE of the ASL device with silicon-based channel/interconnect is maximized. The optimal doping concentration that maximizes

SITE is a function of the interconnect length. This is because the interconnect length relative to the spin-relaxation length determines the exponential signal degradation within the interconnect. The best-case SITE of the ASL device for a 1 μm long Si interconnect is approximately 0.3 at a doping concentration of 3×10^{18} cm^{-3}. This value of SITE is 3× better than the best-case SITE obtained in the case of metallic conductors (see Figure 101).

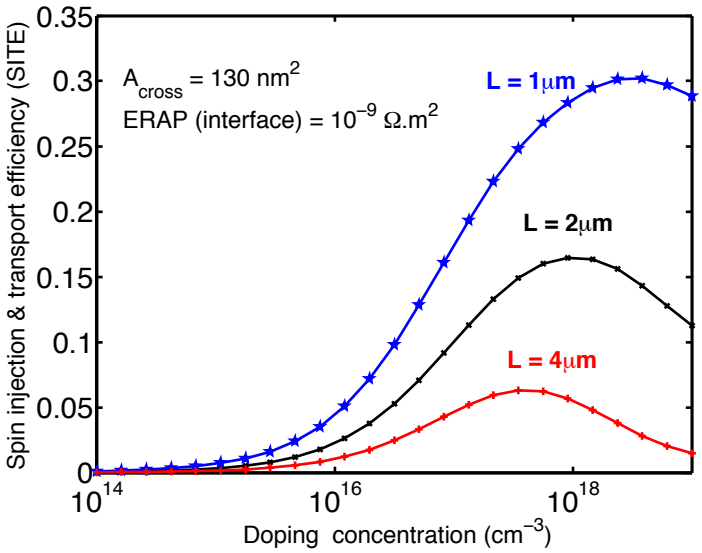

Figure 106: Spin injection and transport efficiency versus doping concentration in an ASL device with a silicon interconnect. Various interconnect lengths are considered.

Figure 107 shows the SITE of an ASL device with GaAs interconnects versus the doping in the interconnect. In the case of bulk GaAs, the spin-relaxation length becomes independent of the doping concentration and saturates to a value of 0.5 μm at R.T. As the doping concentration increases, the SRAP of the GaAs interconnect reduces due to a reduction in the material resistivity and this reduces the conductivity mismatch between the interconnect and the injecting ferromagnet. Hence, the SITE of the ASL device with GaAs interconnects continually improves with an increase in doping concentration for all interconnect lengths. At an interconnect length of 1 μm and a doping concentration of 10^{18} cm^{-3}, it is found that the SITE of the ASL device

with GaAs interconnect is 0.18 at R.T. This value of SITE is lower than that with a 1 μm long Si interconnect at the same doping level and lattice temperature.

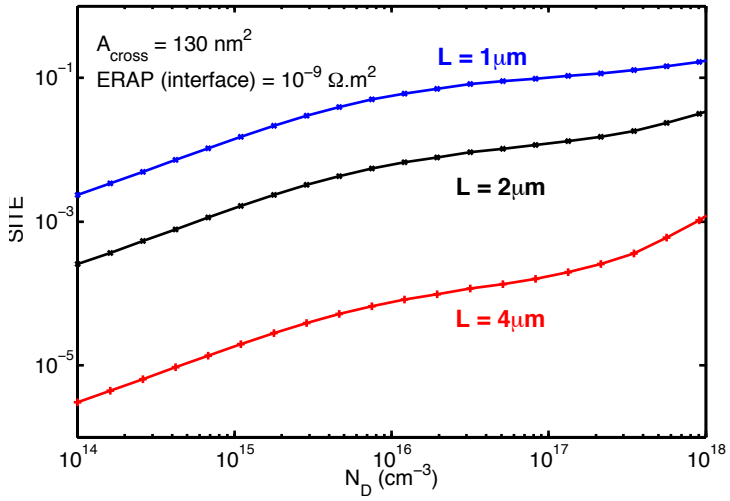

Figure 107: Spin injection and transport efficiency versus doping concentration in ASL device with a GaAs interconnect. Various interconnect lengths are considered.

The SITE of the ASL device with a narrow GaAs interconnect in the presence of quantum confinement effects is shown in Figure 108 for two values of the interconnect length. At an interconnect length of 1 μm and width of 7.5 nm, SITE is 0.09 (denoted by point "a" in Figure 108). If the interconnect is 2 μm long and 7.5 nm wide, the SITE degrades to 0.014 (denoted by point "b" in Figure 108). The SITE for a fixed interconnect length improves with an increase in the interconnect width and saturates to a value of 0.125 for $W > 10$ nm for L = 1 μm. An increase in interconnect length severely degrades SITE particularly for very narrow interconnect widths (< 5 nm).

5.3 Conclusions

For an ASL device, a figure of merit called the spin injection and transport efficiency (SITE) is identified. The SITE captures the losses in the spin signal due to two factors: (i) imperfect injection from the ferromagnet into the interconnect and (ii)

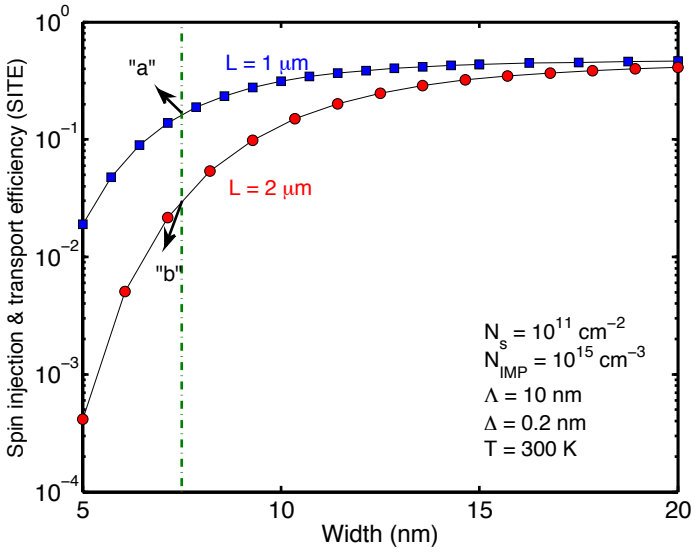

Figure 108: Spin injection and transport efficiency of the ASL versus the interconnect width for a GaAs QW interconnect. Interconnect lengths of 1 μm and 2 μm are considered.

exponential degradation within the interconnect due to spontaneous spin flipping processes. In this chapter, the mathematical formalism to compute SITE in the non-local geometry of the ALS device is presented. The SITE is then evaluated for various interconnect materials in the presence of size effects. It is shown that scaling the cross-sectional dimensions of the ASL device in the presence of size effects leads to a significant degradation in the SITE. A reduction in SITE would lead to an increase in the energy dissipation of the circuit. For an ASL device with a silicon interconnect, there exists an optimal doping concentration that maximizes SITE for given design parameters. However, for an ASL device with a GaAs interconnect, the SITE always increases with an increase in doping concentration. The SITE of an ASL device with GaAs interconnects in the presence of quantum well effects is also evaluated. It is shown that SITE with narrow GaAs interconnects does not show any dependence on interconnect width when the width is greater than 15 nm.

Finally, the findings of this chapter are summarized in Table 27 that shows the

value of SITE of the ASL device with various interconnect materials at an interconnect length of 1 μm and a width of 7.5 nm. The value of the interface ERAP chosen for metallic interconnects is 10^{-12} $\Omega.m^2$ and that for GNR interconnects is 8.45×10^{-12} $\Omega.m^2$ per conduction channel, while for semiconducting interconnects a larger value of 10^{-9} $\Omega.m^2$ is selected to overcome the conductivity mismatch between the semiconductor and the injecting nanomagnet. It can be seen from this table that silicon interconnects have the best-case SITE, while Cu interconnects have the lowest value of SITE. The value of SITE for Cu is very low mainly because of the very short spin-relaxation length in Cu in the presence of size effects.

Table 27: The value of spin injection and transport efficiency in an ASL device with various interconnect materials. The interconnect length is chosen to be 1 μm, and the interconnect width is 7.5 nm.

Material	**SITE**
Copper (R = 0.145, p = 0)	3.06×10^{-4}
Aluminum (R = 0.01, p = 0)	8.9×10^{-3}
GNR (T_{TX}=0.1, T_{RX}=0.5, E_f = 0.2 eV, $P_{GNR} = 0.2$)	0.125
ML-GNR (N=4, T_{TX}=0.1, T_{RX}=0.5, E_f = 0.2 eV, $P_{GNR} = 0.2$, ρ_m = 0.3 $\Omega.m$)	0.25
Silicon ($N_D = 10^{18}$ cm^{-3})	0.286
Gallium Arsenide ($N_D = 10^{17}$ cm^{-3})	0.1
Gallium Arsenide QWs ($N_{IMP} = 10^{14}$ cm^{-3}, $N_s = 10^{10}$ cm^{-2})	0.09

CHAPTER VI

CIRCUIT- AND SYSTEM-LEVEL ANALYSES OF ALL-SPIN LOGIC

In this chapter, the circuit- and system-level issues pertaining to the spin logic with the all-spin logic (ASL) switching element will be identified. First the nanomagnet switching characteristics with two flavors of switching are analyzed. Flavor 1 corresponds to a full spin-torque assisted flipping of the receiver nanomagnet. Flavor 2 is a mixed-mode switching of the nanomagnet utilizing Bennett clocking to align the receiver along its hard axis (HA), while utilizing spin currents to only tip the nanomagnet around the HA towards one of its stable states. Second, the repeater-insertion requirements for overcoming signal losses in the interconnect and for maximizing the performance of the spin circuit are quantified. The input electrical current that minimizes the energy dissipation of a delay-optimized, repeater-inserted spin interconnect is quantified for both full spin-torque and mixed-mode switching schemes of the nanomagnet. Third, the energy-delay product of spin and CMOS circuits are compared. Major differences in the energy-delay tradeoff of the two logic technologies are identified. Fifth, the stochastic wire length distribution models for random logic are used to obtain the average performance and the average energy dissipation of the ASL system, which are then compared against those of its CMOS counterparts. The impact of system size and complexity on the average system performance metrics is also evaluated. Spin repeaters are ubiquitous in spin logic. However, only a certain fraction of the total number of gates in a logic block can be dedicated as repeaters. An upper bound on the circuit size of the ASL system is also obtained as a function of material and design parameters. Finally, the chapter is concluded.

6.1 The spin-torque effect and the nanomagnet dynamics

Spin torque refers to the phenomenon in which a pure spin current can rotate the magnetization of a nanomagnet. The component of the spin angular momentum transverse to the nanomagnet's moment is absorbed by the nanomagnet. If the nanomagnet responds as a single domain, the magnetic moment of the nanomagnet may begin to rotate. To understand the dynamics of the nanomagnet, the effect of various torques acting on the nanomagnet must be considered. The various torques include the torques due to an applied magnetic field, magnetic anisotropies, and the intrinsic damping in the nanomagnet.

In this study, the nanomagnet is assumed to be an elliptical body shown in Figure 109. The magnetization is assumed to lie in the y-z plane. The shape anisotropy energy of the nanomagnet is given as

$$E_{SHA} = \frac{\mu_0}{2} M_s^2 \Omega N_d, \tag{171}$$

where μ_0 is the free-space permeability, M_s is the saturation magnetization of the nanomagnet, Ω is the volume of the nanomagnet, and N_d is the demagnetization factor of the nanomagnet and is expressed as

$$N_d = N_{d,zz} \cos^2(\theta(t)) + N_{d,yy} \sin^2(\theta(t)), \tag{172}$$

where $N_{d,zz}$ and $N_{d,yy}$ are the demagnetization coefficients along the z- and y-axes, respectively. The demagnetization coefficients are a function of the nanomagnet dimensions. If the thickness, l, of the nanomagnet is much smaller than both the major-axis dimension, a, and the minor-axis dimension, b, the demagnetization coefficients can be given as [187]

$$N_{d,zz} = \frac{\pi}{4}\left(\frac{l}{a}\right)\left(1 - \frac{1}{4}\left(\frac{a-b}{a}\right) - \frac{3}{16}\left(\frac{a-b}{a}\right)^2\right), \tag{173}$$

$$N_{d,yy} = \frac{\pi}{4}\left(\frac{l}{a}\right)\left(1 + \frac{5}{4}\left(\frac{a-b}{a}\right) + \frac{21}{16}\left(\frac{a-b}{a}\right)^2\right). \tag{174}$$

It can be seen from the above set of equations that the nanomagnet magnetization will prefer to be oriented along the easy axis because it minimizes the shape anisotropy energy of the nanomagnet. Hence, $\theta = 0$ and $\theta = \pi$ points on the energy landscape are collectively referred to as the easy axis (EA), which is assumed to be the z-axis.

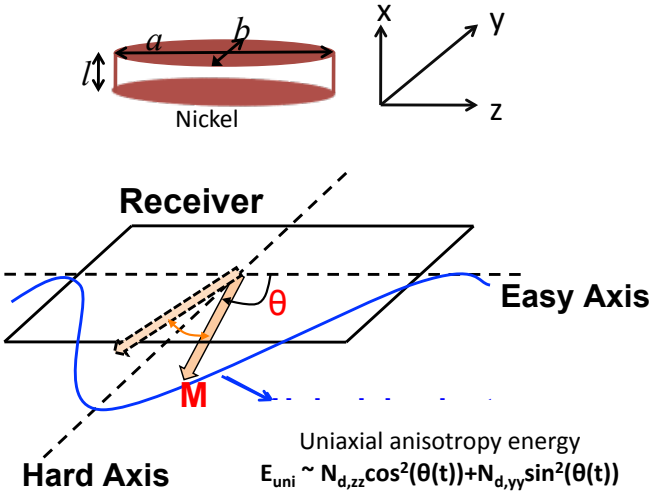

Figure 109: The top figure shows the elliptical nanomagnet with the coordinate axes. The major-axis dimension of the nanomagnet is denoted as a, the minor-axis dimension is denoted as b, while the thickness of the nanomagnet is denoted as l. The bottom figure is the shape anisotropy energy landscape of the nanomagnet.

In the spherical coordinates, the torque acting on the nanomagnet within a unit volume due to the shape anisotropy is given as

$$\tau_{SHA}(t) = -\vec{n}_m(t) \times \nabla E_{SHA}(\theta(t)), \tag{175}$$

where $\vec{n}_m(t) = \vec{M}(t)/|\vec{M}(t)|$ is the instantaneous unit vector along the direction of magnetization of the nanomagnet. Using $E_{SHA}(t)$ from Eq. (171), the torque due to shape anisotropy can be expressed as

$$\tau_{SHA}(t) = -2B_0 \sin(\theta(t))\cos(\theta(t))\widehat{e_\phi}, \tag{176}$$

where $B_0 = \frac{\mu_0}{2} M_s^2 \Omega\,(N_{d,zz} - N_{d,yy})$, and $\widehat{e_\phi}$ is the unit vector along the ϕ direction. It can be seen from Eq. (176) that the torque due to shape anisotropy vanishes when

$\theta(t) = 0$ or $\theta(t) = \pi/2$. Hence, $\theta = 0$ and $\theta = \pi/2$ are referred to as the "stagnation points". Typically, the nanomagnet magnetization will never be exactly along the easy axis due to thermal noise. Hence, $\theta = 0$ and $\theta = \pi/2$ points in the nanomagnet dynamics are avoided.

The torque on the nanomagnet due to the spin transfer torque is given as

$$\tau_{STT}(t) = -s\vec{n}_m(t) \times (a'\vec{n}_m(t) + b'\vec{n}_s(t) + c'(\vec{n}_m(t) \times \vec{n}_s(t))), \tag{177}$$

where $s = (\hbar/2e)\eta I_{elec}$ is the spin angular momentum deposition per unit time, and η is the spin injection and transport efficiency, b' and c' are dimensionless voltage-dependent parameters, while a' is irrelevant in this context as the spin-torque term containing a' vanishes. Assuming that the spin polarization subtends an angle ζ with the positive z-axis, the spin-transfer torque in spherical coordinates may be given as

$$\tau_{STT}(t) = s\,(-b'(V)sin(\zeta - \theta(t))\widehat{e_\phi} + c'(V)sin(\zeta - \theta(t))\widehat{e_\theta}). \tag{178}$$

The dynamics of the nanomagnet under various torques can be modeled using the Landau-Lifshitz-Gilbert (LLG) equation given as

$$\frac{d\vec{n}_m(t)}{dt} + \alpha\left(\vec{n}_m(t) \times \frac{d\vec{n}_m(t)}{dt}\right) = \frac{\gamma}{M_V}(\tau_{SHA}(t) + \tau_{STT}(t)), \tag{179}$$

where α is the dimensionless phenomenological Gilbert damping constant, γ is the gyromagnetic ratio for electrons, and $M_V = \mu_0 M_s \Omega$. There are two flavors of nanomagnet switching that we consider in this analysis: (i) full spin-torque-assisted switching (STS) and (ii) mixed-mode switching (MMS).

6.1.1 Full spin-torque assisted switching (STS)

In the STS mode of nanomagnet switching, it is assumed that the nanomagnet is initially oriented oriented along its easy axis (i.e. $\theta \to \pi$). The spin polarization is assumed to be oriented along the z-axis, i.e., $\zeta = 0$. The time taken by the incoming spin current to rotate the nanomagnet from $\theta \approx \pi$ to $\theta \approx 0$ is obtained by solving

the LLG equation (Eq. (179)). The compact expression of the nanomagnet delay as obtained in [187] is

$$\tau_{STS} = -\frac{1+\alpha^2}{2\gamma\alpha B_0}\mu_0 M_s \Omega \frac{m}{m^2-1}\left(m\ln\left(\frac{1-m\cos(\nu)}{1+m\cos(\nu)}\right) - \ln\left(\frac{1-\cos(\nu)}{1+\cos(\nu)}\right)\right), \quad (180)$$

where $m = 2\alpha B_0/s$. The above equation is valid for $m \leq 1$, which means that there is a lower bound on the electrical current in the transmitter for which a spin-torque-assisted flipping of the nanomagnet would take place. The minimum required electrical current is mathematically given as

$$I_{elec}(min) = \frac{\alpha}{\eta}\frac{4qB_0}{\hbar}, \quad (181)$$

where η is the spin injection and transport efficiency (SITE) of the ASL circuit (see Chapter V). There is an optimum size of the receiver nanomagnet to minimize its switching time. The impact of the nanomagnet volume is tied to both its switching time and its thermal stability. Keeping the thermal stability of the nanomagnet fixed, the optimum dimensions of the nanomagnet to minimize its switching time are obtained by minimizing the function

$$f = \frac{\Omega}{N_{d,yy} - N_{d,zz}}. \quad (182)$$

The switching time versus the minor axis dimension is plotted in Figure 110. The inset plot of Figure 110 shows the switching delay versus the ratio, a/b, of the major-axis to minor-axis dimension. Clearly there is an optimum value of a/b that minimizes the switching delay of the nanomagnet. The ratio of the major and the minor axis dimension that minimizes the delay is $a/b = 1.65$. This result is independent of the barrier height, the nanomagnet thickness, and the value of m. The material and design properties of the nanomagnet used for future simulations are provided in Table 28.

Choosing the material and design parameters to yield a $3k_BT$ thermal stability of the nanomagnet, the delay associated with STS mode is shown in Figure 111. The STS

mode delay is large for a small value of ν; this means that it is difficult for a pure spin current to induce a torque on the nanomagnet if the nanomagnet is aligned close to the EA. However, as the nanomagnet magnetization moves closer to the HA, it becomes easier for the spin current to rotate the nanomagnet magnetization. The inset plot of Figure 111 shows the impact of increasing the input spin current, $I_{spin,inp}$, to induce spin-torque-assisted switching of the nanomagnet. As the input current increases, the over-drive of spin current available at the nanomagnet increases making it easier for the spin current to switch the nanomagnet magnetization. However, the improvement in the nanomagnet delay saturates with increasing $I_{spin,inp}$.

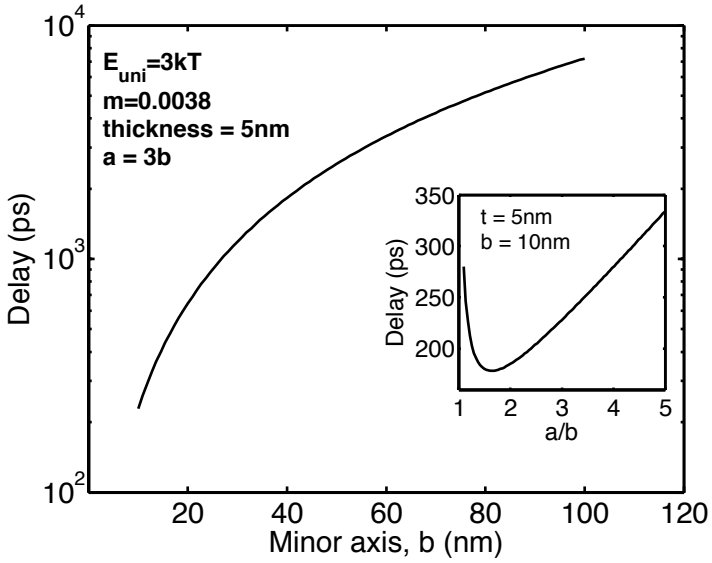

Figure 110: Switching time of the nanomagnet versus the dimension of its minor axis. The inset shows that there is a minimum in the switching time of the nanomagnet versus the ratio of the major and the minor axis (ratio = a/b).

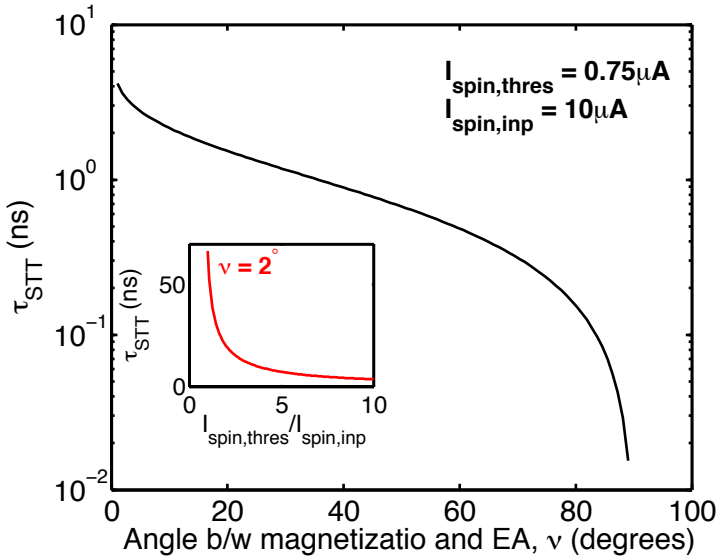

Figure 111: The STS delay of the nanomagnet versus the angle between the nanomagnet magnetization and the EA. The inset plot shows the STS mode delay of the nanomagnet versus the input spin current.

Table 28: Material and design parameters of the nanomagnet (nickel).

Parameter	**Value**
Major-axis of the elliptical nanomagnet, a	16.5 nm
Minor-axis of the elliptical nanomagnet, b	10 nm
Thickness of the nanomagnet, l	5 nm
Saturation magnetization M_s	$3.93\times\ 10^5$ A/m
Damping coefficient, α	0.01
Uniaxial shape anisotropy, E_{uni}	$3k_BT$
Threshold current of the receiver nanomagnet, $I_{spin,thres}$	0.75μA

6.1.2 Mixed-mode switching (MMS)

In the MMS mode, an external clock signal is used to align the nanomagnet along its HA, which is only a marginally stable state of the nanomagnet. This supports the Bennett clocking scheme for the nanomagnet-based logic. There are a few innovative ways to rotate the magnet from its EA to the HA and provide a metastable quiescent point. These possible schemes are:

1. use of voltage-generated stress (VGS) in a multiferroic magnet consisting of a magnetostrictive layer (Nickel) and a piezoelectric layer to rotate the nanomagnet from $(\pi - \nu)$ to $(\pi - \phi)$, where $\phi < \pi/2$.

2. applying a voltage to a fixed magnetic layer in contact with the output layer through a spacer region; the spacer region accumulates spins in the direction of the fixed layer and helps to exert spin torque on the output nanomagnet.

In the MMS mode, the switching is accomplished in three distinct phases. In Phase 1, the nanomagnet is aligned along its HA using Bennett clocking. In Phase 2, the spin current through the nanomagnet is switched on and the nanomagnet magnetization rotates from $(180 - \nu)^\circ$ to ν°, where ν° is slightly smaller than 90°. In the last phase, the spin torque current is switched off and the intrinsic damping of the nanomagnet brings the magnetization to its stable orientation. The delay associated with switching the nanomagnet using the MMS mode is shown in Figure 112 as a function of the ratio of the threshold current of the nanomagnet and the input spin current. The switching delay of the nanomagnet using MMS mode is much lower than that using STS mode. Further, the delay of the MMS mode also saturates with an increase in the overdrive of the nanomagnet, i.e., an increase in the ratio $I_{spin,thres}/I_{spin,inp}$.

While the STS flavor of nanomagnet switching has a simpler clocking scheme, the MMS flavor of the nanomagnet switching may be more energy efficient as it can

significantly reduce the time duration for which the electrical current needs to be switched on. The process of aligning the nanomagnet along its HA may be done in parallel with other computations in the system. For instance, the receiver nanomagnet may already be aligned along the HA at the time the spin current reaches it. This can help to mask the delay of rotating the nanomagnet from the EA to the HA. Once the magnetization of the nanomagnet tips towards its stable axis, the spin current is switched off. At this point, either the intrinsic damping in the nanomagnet may help to rotate the magnetization all the way to the stable state or it may be assisted by stress in the case of VGS switching scheme.

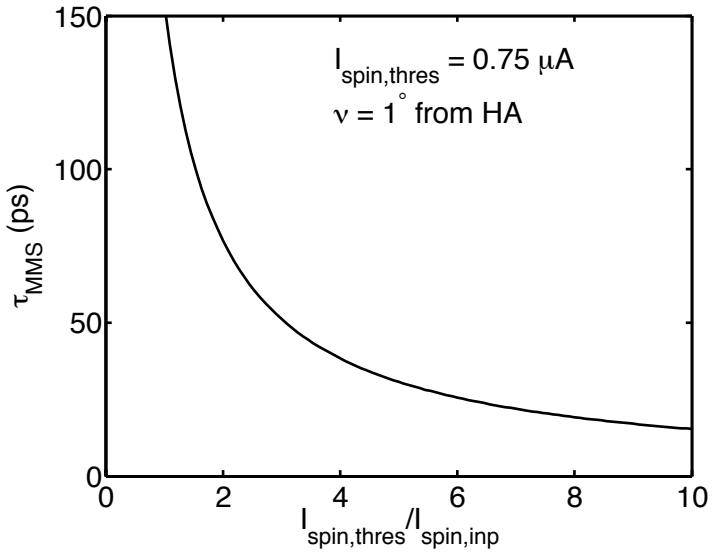

Figure 112: Switching delay of the nanomagnet using the MMS mode. The nanomagnet magnetization is initially aligned at an angle of 1° from the HA.

6.2 Repeater-insertion requirements

In the ASL device, only a certain fraction of the input electrical current reaches the receiver. That is to say, the SITE in the circuit is less than the conductivity polarization of the injecting ferromagnet. Further, the SITE degrades with an increase in the interconnect length as discussed in Chapter V. A reduction in the value of SITE

means that there is a degradation in the overdrive at the receiver nanomagnet. This can severely degrade the switching of the nanomagnet, particularly in the case of full spin-torque-assisted switching. The impact of the interconnect length on increasing the switching time of the nanomagnet is shown in Figure 113.

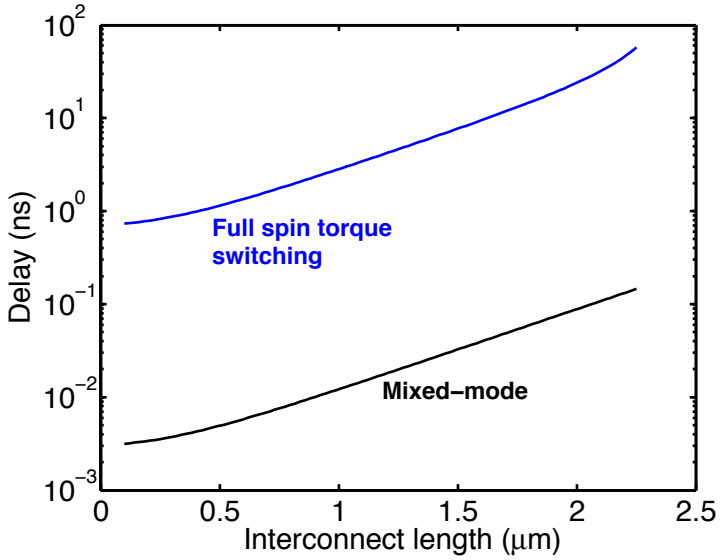

Figure 113: Switching delay of the nanomagnet versus the interconnect length. The simulation parameters are the same as shown in Figure 100. The electrical resistance area product (ERAP) of the transmitting interface in the ASL device is taken to be $10^{-12}\ \Omega.m^2$, and the spin-relaxation length is taken to be 0.5 μm.

It can be seen from Figure 113 that as the interconnect length increases, the response of the nanomagnet for both STS and MMS modes of switching becomes sluggish. However, the impact of the interconnect length on the switching of the MMS mode is less drastic than that in the case of STS mode. For an increase in the interconnect length from 0.1 μm to 2.25 μm, the delay of the STS mode increases from 0.73 ns to 57 ns; this corresponds to an 80× increase in the delay. For the same simulation parameters, the delay of the MMS mode increases from 3.16 ps to 145 ps; this corresponds to 45× increase in the delay.

6.2.1 Critical interconnect length

A critical interconnect length, L_{crit}, is defined such that for for an interconnect length $L > L_{crit}$, the spin signal at the receiver end does not reach the receiver threshold ($I_{spin,thres}$). The critical interconnect length is a function of the receiver sensitivity given by the ratio $I_{elec}/I_{spin,thres}$, the material parameters of the interconnect and the interface characteristics. Figures 114 - 117 show the critical interconnect length as a function of the inverse of receiver sensitivity, which is denoted as "r" in the figures. As r increases or the receiver sensitivity drops, the critical interconnect length degrades significantly for all interconnect materials. The presence of size effects also degrades the critical interconnect length drastically for metallic interconnects. Further, the critical interconnect length for Al is slightly better than that in the case of Cu. This is because of a superior spin-relaxation length in Al than in Cu.

For GaAs interconnects, an increase in the doping concentration improves the critical interconnect length at all values of the doping concentration. This is because an increase in doping concentration improves conductivity of GaAs without degrading its spin-relaxation length. Hence, an increase in doping improves the spin-injection efficiency into the interconnect, which further improves the critical interconnect length in the case of GaAs. In the case of Si interconnects, an increase in doping may not necessarily improve the critical interconnect length for all values of the receiver sensitivity. While the conductivity of Si improves with doping, the spin-relaxation length is adversely affected. Hence, the critical interconnect length may increase or decrease with the doping density for a given value of the receiver sensitivity. For GaAs QWs, an increase in N_s improves L_{crit}. However, this may only be true so long as the increase in N_s does not lead to band to band scatterings.

In the case of GNR interconnects, an increase in the transmission coefficient, T_{TX}, at the transmitter terminal severely limits the critical interconnect length. This results from the fact that an increase in T_{TX} reduces the spin filtering of electrons through

the interface between the interconnect and the ferromagnet. In addition, amongst all the interconnects explored here, GNRs offer the longest critical interconnect length at all values of r for $T_{TX} = 0.1$.

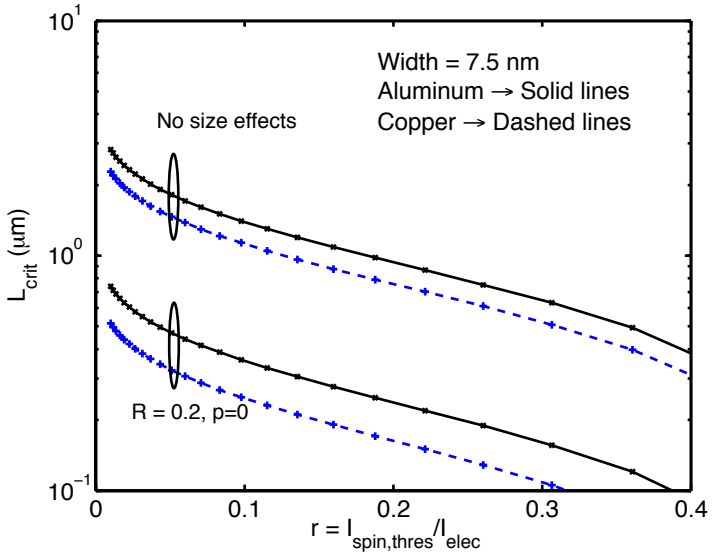

Figure 114: Critical interconnect length for **metallic interconnects** as a function of inverse of receiver sensitivity.

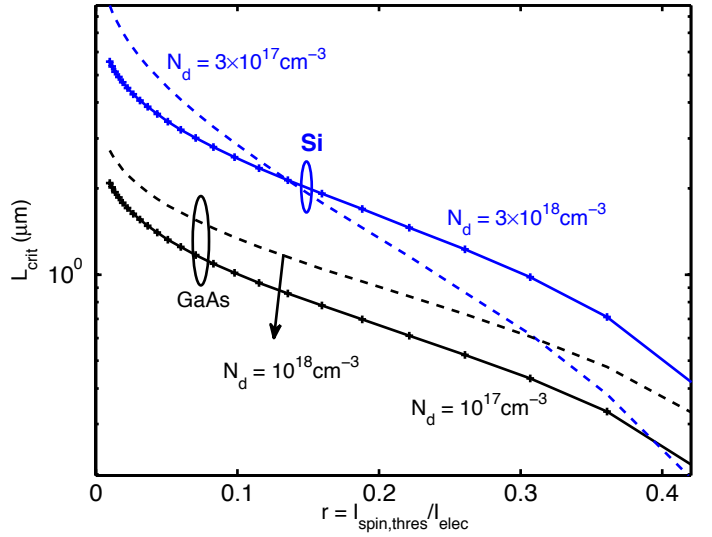

Figure 115: Critical interconnect length for **semiconducting interconnects** as a function of inverse of receiver sensitivity.

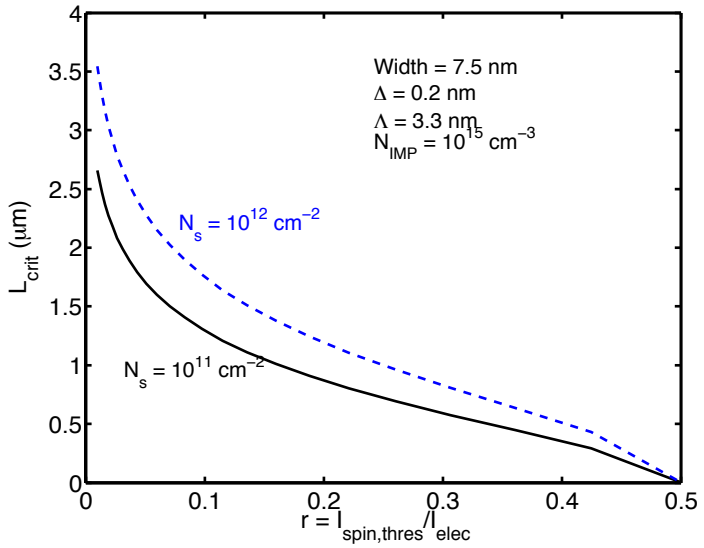

Figure 116: Critical interconnect length for **GaAs quantum well interconnects** as a function of inverse of receiver sensitivity.

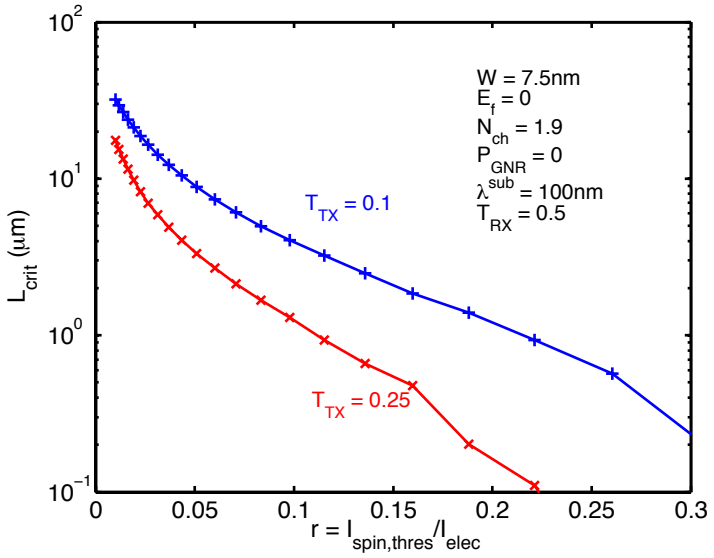

Figure 117: Critical interconnect length for **graphene nanoribbon interconnects** as a function of inverse of receiver sensitivity.

6.2.2 Optimal repeater-insertion frequency

For an interconnect length longer than the critical interconnect length, spin repeaters are required to be inserted along the interconnect. However, since the delay of the spin interconnect is a quadratic function of the interconnect length, spin repeaters may also be inserted to minimize the delay of the interconnect. The delay of a repeater-inserted spin interconnect is given as

$$t_{INT,rep} = \left(\frac{(L/m_{seg})^2}{2D} + \frac{L/m_{seg}}{v_f} + t_{rep} \right) m_{seg}, \tag{183}$$

where m_{seg} is the number of segments along the interconnect. If repeaters are inserted to account for signal losses in the interconnect, the number of segments, m_{seg}^{crit}, is given as

$$m_{seg}^{crit} = \left[\frac{L}{L_{crit}} \right] + 1. \tag{184}$$

The optimal number of segments that minimize the interconnect delay can be found by solving the equation

$$\frac{\partial t_{INT}}{\partial m_{seg}} \left(m_{seg}^{opt} \right) = 0. \tag{185}$$

In Figure 118, we show the delay versus the ratio of the segment length and the critical length for a Cu interconnect. It can be clearly seen from this figure that the delay of the interconnect is minimized at a segment length that is smaller than the critical interconnect length. Hence the optimal number of segments along the interconnect to minimize the interconnect delay will be greater than or equal to the critical number of segments along the interconnect length. Further, the delay of the interconnect around the optimal point does not change very drastically. That is to say, in this example for L_{seg}/L_{crit} between 0.4 and 0.6, the delay does not change very drastically for the STS mode of the nanomagnet dynamics. For the MMS mode as shown in the inset plot of Figure 118, the optimal number of segments that minimize

the delay will be very close to the critical number of segments. This is because in the MMS mode of nanomagnet switching, the time constant of the nanomagnet depends weakly upon the overdrive available at the nanomagnet. Even in the MMS mode, the delay landscape around the optimal point is relatively flat.

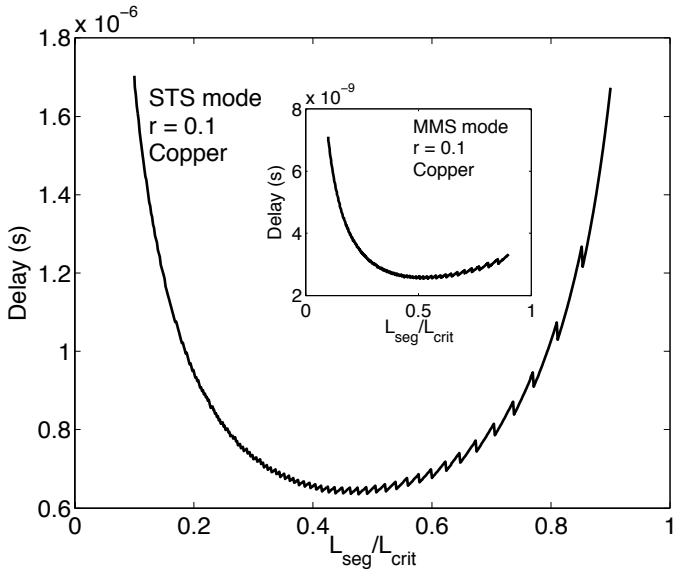

Figure 118: A representative plot showing that the optimal number of segments to minimize the delay of the spin interconnect will generally be slightly more than the critical number of segments.

In Figures 119-122, the ratio of optimal number of segments and the critical number of segments along metallic interconnects as a function of the ratio r is plotted. The interconnect width is taken to be 7.5 nm. Various interconnect lengths are considered. Both MMS and STS modes for the nanomagnet dynamics are considered. It can be seen from these figures that the interconnect length does not significantly influence the ratio $\mathrm{m}_{\mathrm{seg}}^{\mathrm{opt}}/\mathrm{m}_{\mathrm{seg}}^{\mathrm{crit}}$. Further, for MMS mode, the ratio $\mathrm{m}_{\mathrm{seg}}^{\mathrm{opt}}/\mathrm{m}_{\mathrm{seg}}^{\mathrm{crit}}$ saturates to ≈ 1.1 for $\mathrm{r} > 0.2$. Likewise for STS mode, the ratio $\mathrm{m}_{\mathrm{seg}}^{\mathrm{opt}}/\mathrm{m}_{\mathrm{seg}}^{\mathrm{crit}}$ saturates to ≈ 1.6 for $\mathrm{r} > 0.2$. The fact that interconnect length does not drastically influence the optimal number of segments would help us to choose a constant repeater-insertion frequency for the design when the input electrical current $\mathrm{I}_{\mathrm{elec}}$ is less than $5\times$ the

spin threshold current, $I_{spin,thres}$, such that $r > 0.2$.

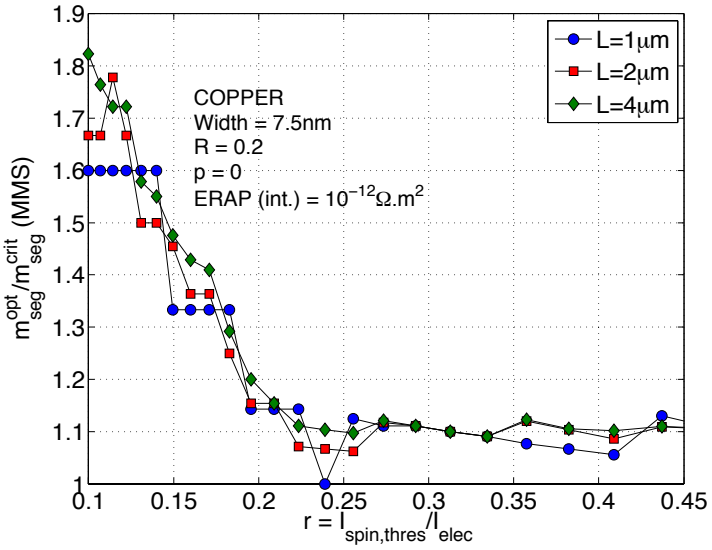

Figure 119: Ratio of optimal number of segments and critical number of segments along Cu interconnect. Mixed-mode switching of the nanomagnet is considered.

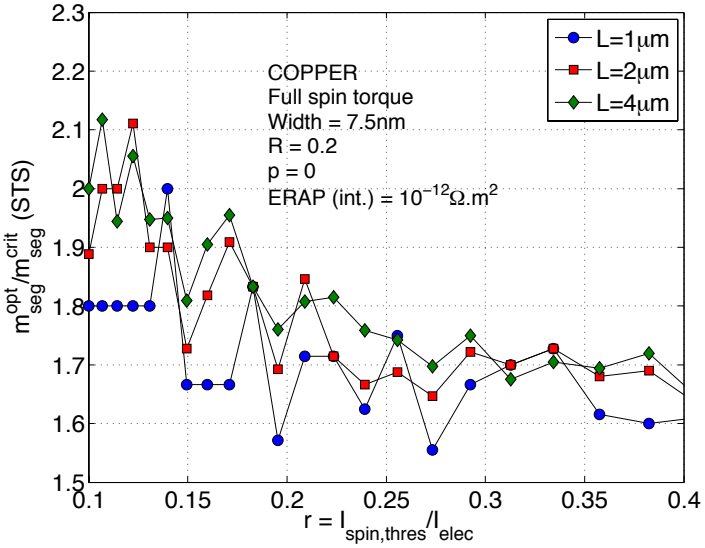

Figure 120: Ratio of optimal number of segments and critical number of segments along Cu interconnect. Full spin-torque switching of the nanomagnet is considered.

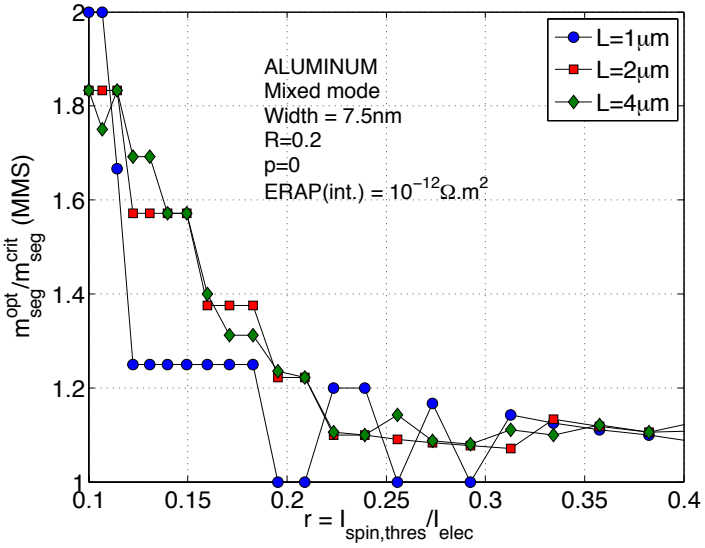

Figure 121: Ratio of optimal number of segments and critical number of segments along Al interconnect. Mixed-mode switching of the nanomagnet is considered.

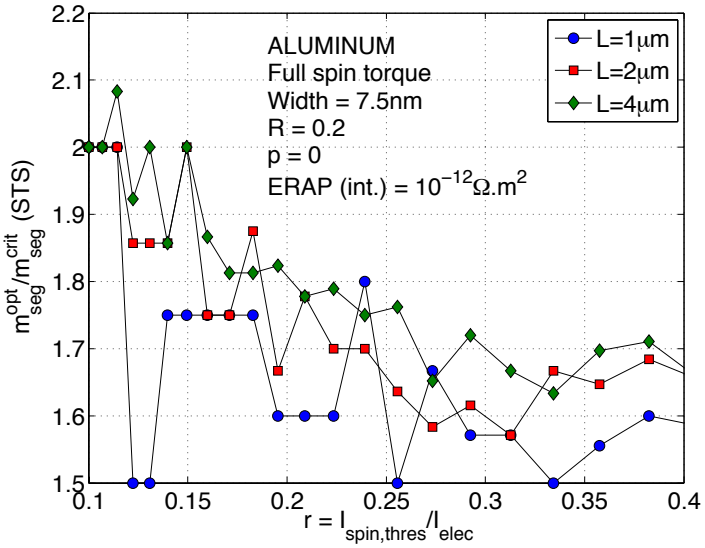

Figure 122: Ratio of optimal number of segments and critical number of segments along Al interconnect. Full spin-torque switching of the nanomagnet is considered.

For semiconducting interconnects, the ratio $m_{seg}^{opt}/m_{seg}^{crit}$ is plotted in Figures 123-126 as a function of the inverse of receiver sensitivity. Various interconnect lengths are considered. Both MMS and STS modes of nanomagnet dynamics have been considered. Similar to the case of metallic interconnects, the interconnect length does

not change the optimal repeater insertion frequency relative to the critical repeater insertion frequency significantly. This is true particularly when $r > 0.2$.

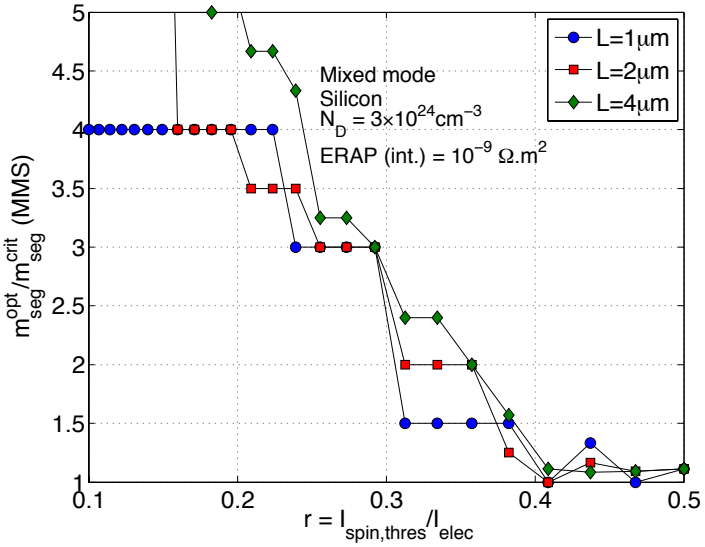

Figure 123: Ratio of optimal number of segments and critical number of segments along Si interconnect. Mixed-mode switching of the nanomagnet is considered.

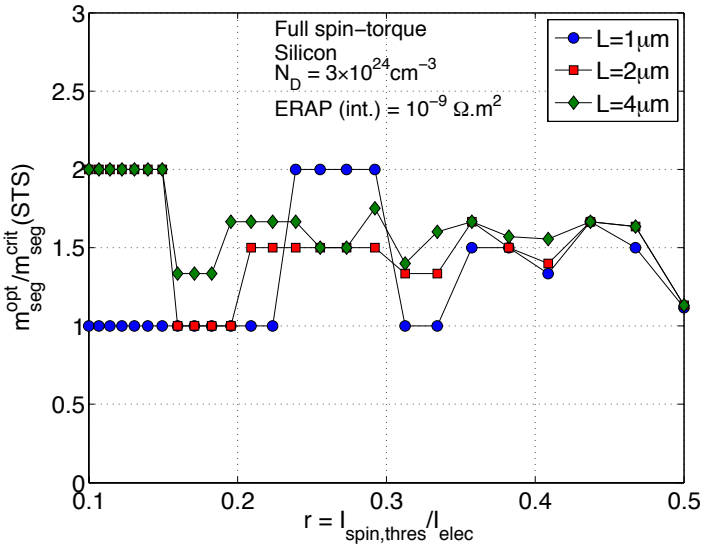

Figure 124: Ratio of optimal number of segments and critical number of segments along Si interconnect. Full spin-torque switching of the nanomagnet is considered.

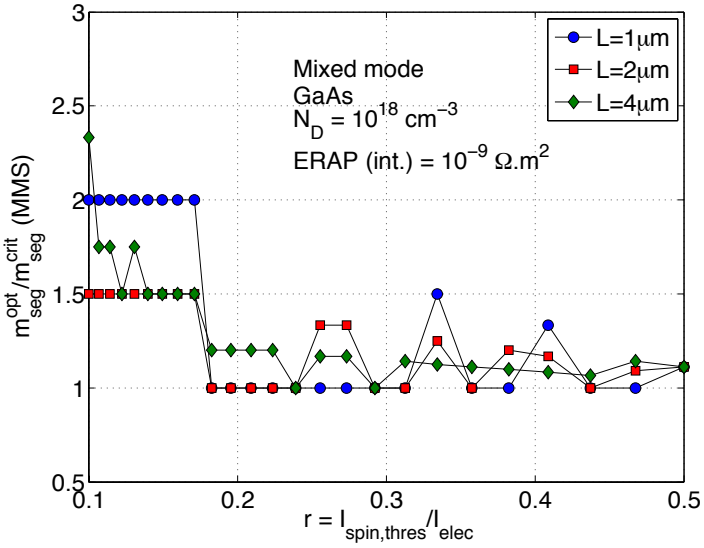

Figure 125: Ratio of optimal number of segments and critical number of segments along GaAs interconnect. Mixed-mode switching of the nanomagnet is considered.

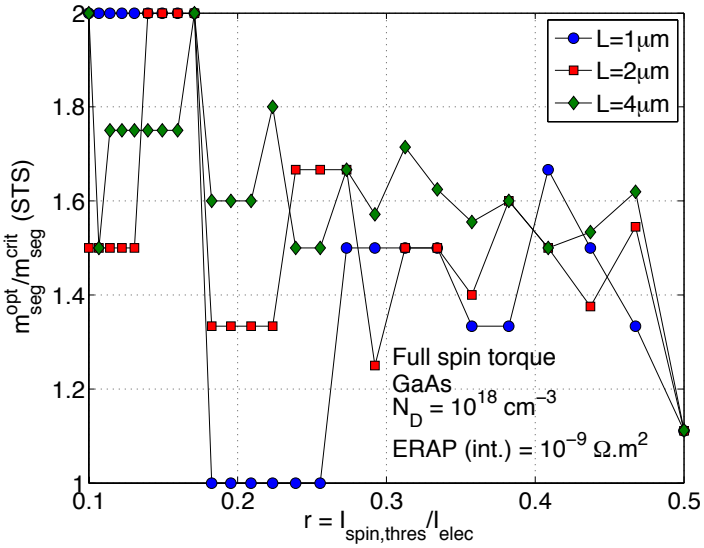

Figure 126: Ratio of optimal number of segments and critical number of segments along GaAs interconnect. Full spin-torque switching of the nanomagnet is considered.

The impact of doping concentration on the optimal repeater-insertion frequency along silicon interconnects is shown in Figure 127. For the STS mode, the ratio $m_{seg}^{opt}/m_{seg}^{crit}$ is nearly independent of the doping concentration for the values of r considered in the analysis. In this case, $m_{seg}^{opt}/m_{seg}^{crit}$ is $\approx$ 1.5-2 for all values of N_d.

However, for the MMS mode, the ratio $m_{seg}^{opt}/m_{seg}^{crit}$ slightly increases with N_d, when $N_d > 10^{17}$ cm^{-3} particularly when $r = 0.2$.

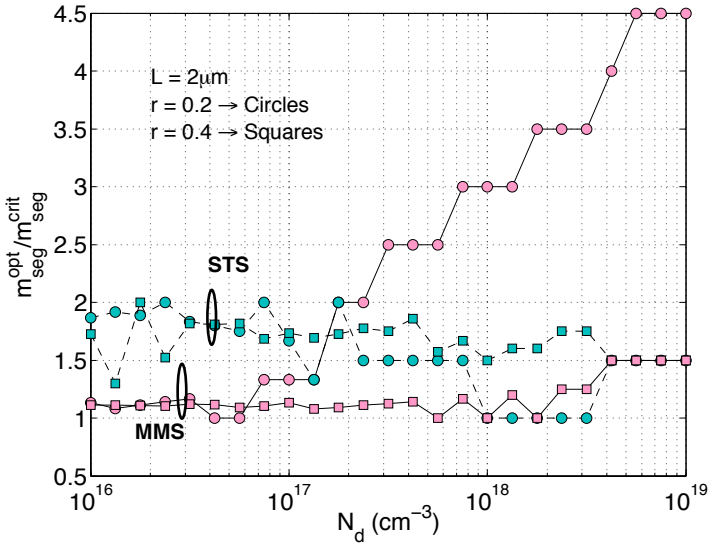

Figure 127: The impact of doping concentration on the optimal number of segments relative to the critical number of segments for a silicon interconnect. Here, r is the inverse of the receiver sensitivity.

The ratio $m_{seg}^{opt}/m_{seg}^{crit}$ versus the inverse of receiver sensitivity for GaAs quantum well interconnects is shown in Figures 128 and 129. For MMS switching, the optimal number of repeaters is the same as the critical number of repeaters for $r > 0.2$. For STS switching, the optimal repeater frequency is 1.5× the critical number of segments for $r > 0.2$ for all interconnect lengths considered in the analysis.

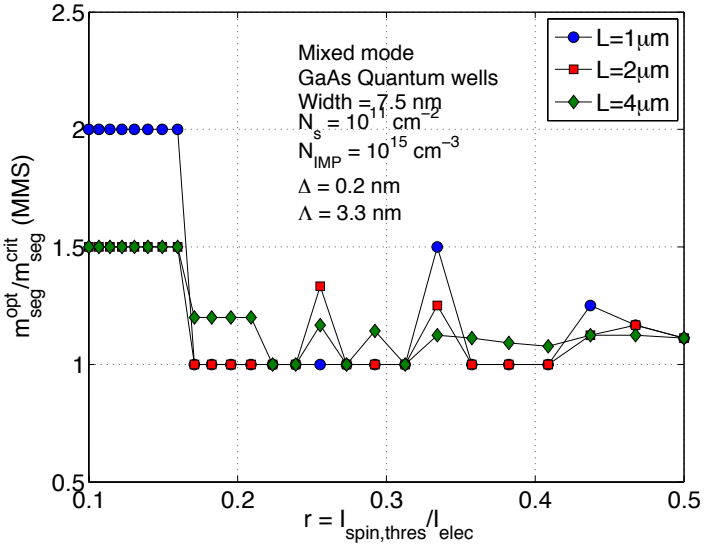

Figure 128: Ratio of optimal number of segments and critical number of segments along GaAs QW interconnect. Mixed-mode switching of the nanomagnet is considered.

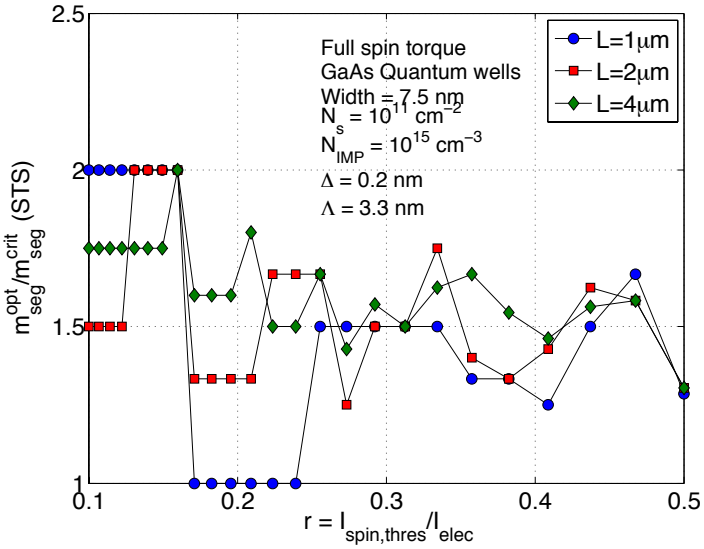

Figure 129: Ratio of optimal number of segments and critical number of segments along GaAs QW interconnect. Full spin-torque switching of the nanomagnet is considered.

The ratio $\mathfrak{m}_{seg}^{opt}/\mathfrak{m}_{seg}^{crit}$ versus the inverse of receiver sensitivity for graphene nanoribbons is shown in Figures 130 and 131. As in the case of other interconnects, the ratio $\mathfrak{m}_{seg}^{opt}/\mathfrak{m}_{seg}^{crit}$ for GNR interconnects is only weakly dependent on the interconnect

length, and it is close to unity for MMS mode. In the case of STS mode, the ratio is close to 1.5.

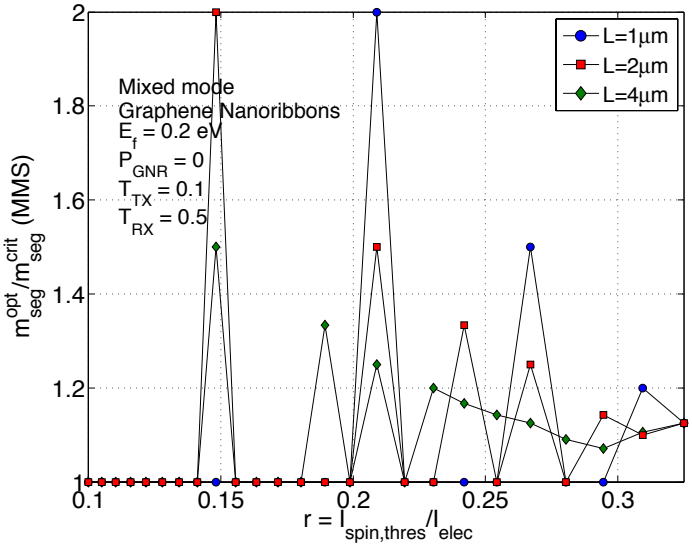

Figure 130: Ratio of optimal number of segments and critical number of segments along a GNR interconnect. Mixed-mode switching of the nanomagnet is considered.

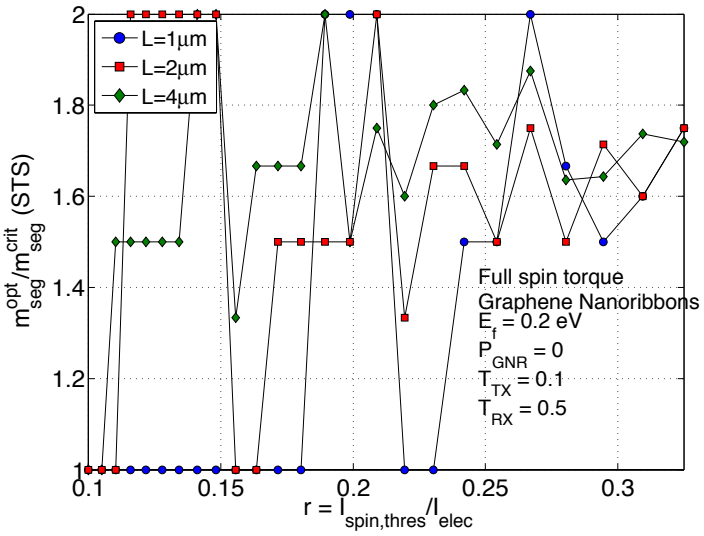

Figure 131: Ratio of optimal number of segments and critical number of segments along a GNR interconnect. Full spin-torque switching of the nanomagnet is considered.

6.3 Energy versus delay

The energy-delay landscape in a CMOS system is shown in Figure 132. The simulation was performed using PETE, an online simulator from NANOHUB[1]. The channel length of the MOS device is taken to be 32 nm. As the supply voltage is scaled down, the energy dissipation of the system reduces quadratically, while the delay of the system increases. However, once the supply voltage becomes much closer to the threshold voltage of the device, the delay increases substantially without an equivalent reduction in the energy dissipation.

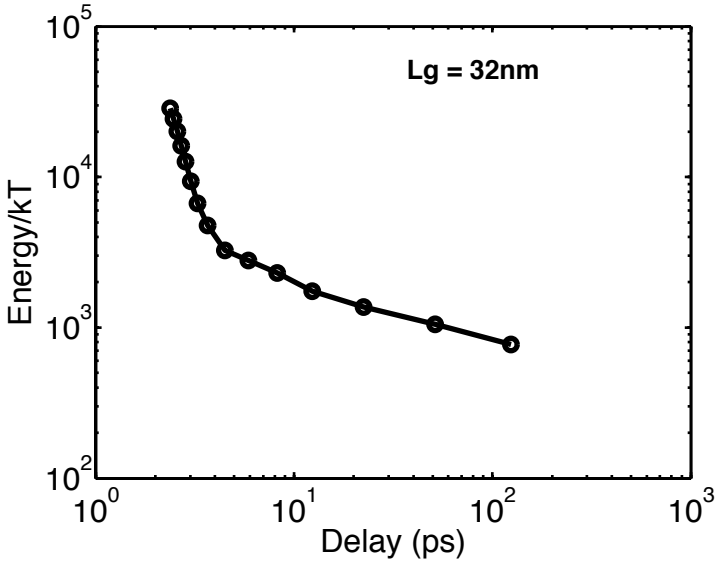

Figure 132: Energy versus delay landscape of the CMOS system. Simulation conducted for a MOSFET with 32 nm channel length.

To obtain the delay versus energy landscape of the ASL circuit, the input electrical current is changed relative to the spin threshold current of the receiver nanomagnet. In Figure 133, the energy dissipation of the ASL circuit with metallic interconnects is plotted as a function of the ratio of the spin threshold current and the electrical current for both STS and MMS modes of nanomagnet dynamics. The energy dissipation is

[1] www.nanohub.org

minimized for $r \approx 0.25$ for the STS mode, irrespective of the interconnect length and the size-effect parameters. For the MMS mode, the energy dissipation becomes relatively flat with r for $r \geq 0.25$. However, a minimum energy point is found to exist for $r \approx$ (0.3-0.4) in the MMS mode. The optimal point for the MMS mode is also found to be independent of the interconnect length and size-effect parameters.

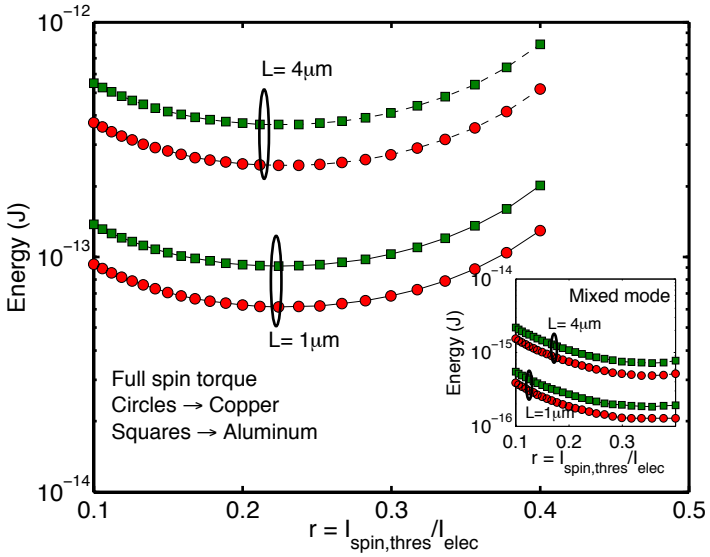

Figure 133: Energy dissipation of the ASL circuit with metallic interconnects as a function of r for the STS mode. The inset plot shows the energy dissipation for the MMS mode.

The energy dissipation of the ASL circuit with semiconducting interconnects is shown in Figure 134 as a function of the ratio r for both STS and MMS modes. The doping concentration selected for the simulation is also shown in the figure. The value of r that minimizes the energy dissipation is plotted in Figure 135 as a function of doping concentration for silicon. For STS mode, the optimal value of $r \approx 0.2$ for doping concentrations in the vicinity of 10^{18} cm^{-3}. For MMS mode, the optimal value of r is $\approx$ (0.3-0.4) for N_d in the vicinity of 10^{18} cm^{-3}. This optimal value of r in the case of semiconducting interconnects with $N_d \approx 10^{18}$ cm^{-3} is the same as that for metallic interconnects in the both STS and MMS modes.

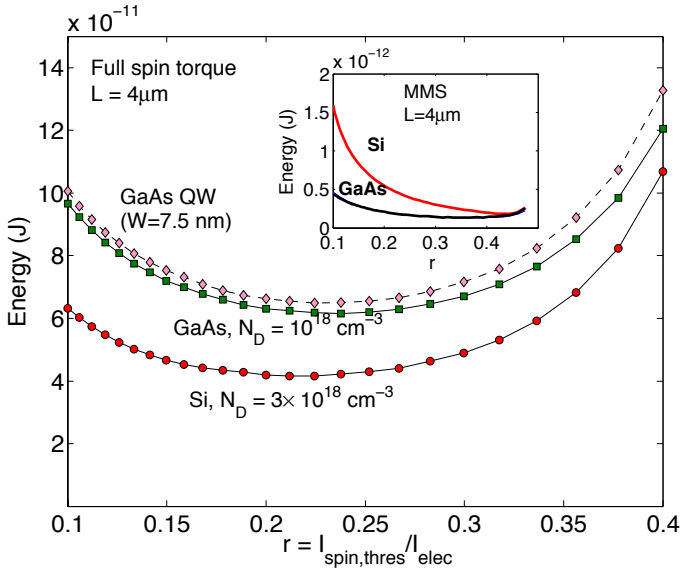

Figure 134: Energy dissipation of the ASL circuit with semiconducting interconnects versus the ratio r for STS mode. The inset plot shows the energy dissipation for the MMS mode.

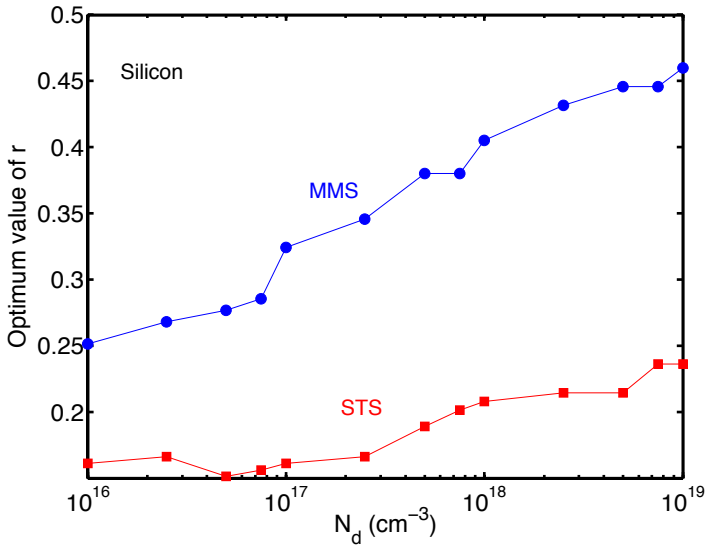

Figure 135: The optimal value of r to minimize the energy dissipation versus the doping concentration for silicon interconnects.

The energy dissipation of the ASL circuit with GNR interconnects is shown as a function of $\mathtt{r}$ in Figure 136. The energy versus $\mathtt{r}$ landscape is relatively flat for STS mode if $\mathtt{r} < 0.2$. The optimal value of $\mathtt{r}$ that minimizes the energy dissipation is equal to 0.15 for STS mode and is ≈ 0.2 for the MMS mode. The interconnect length does not change the optimal point.

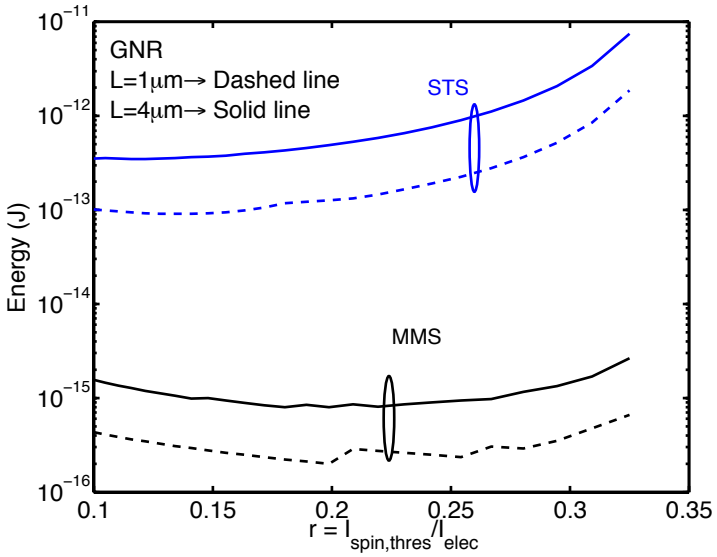

Figure 136: Energy dissipation of the ASL circuit with GNR interconnects.

There exists a minima in the energy-delay landscape of the ASL circuit. This can be explained by using the results shown in Figures 133-136. As the electrical current is scaled down, there is a reduction in the Joule heating in the transmitter but the delay of the ASL circuit increases due to a reduction in the overdrive of the receiver nanomagnet. As the energy dissipation of the ASL circuit is given by the product of the Joule heating and the delay of the circuit, the energy versus delay landscape of the ASL circuit exhibits a minimum (see Figure 137). The minimum point in the energy-delay landscape will depend upon the dynamics, material, and size of the nanomagnet, the interconnect material and the design of the ASL circuit.

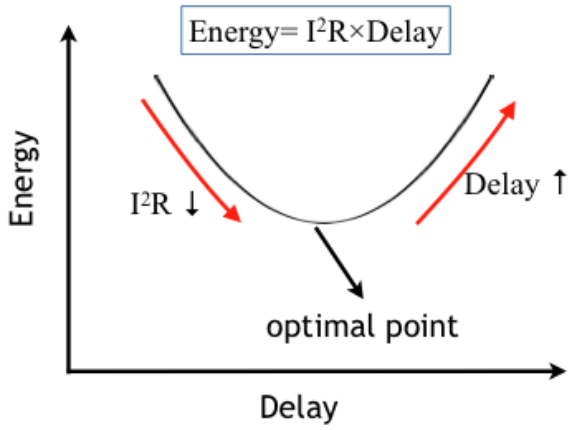

Figure 137: An illustration of the energy-delay landscape of the ASL circuit. There exists a minima in this landscape.

6.3.1 Performance and energy factors of ASL circuit

The performance and the energy factors of the ASL circuit with various interconnects are tabulated in Tables 29 and 30, respectively. The electric current for the STS mode is taken to be 5× the spin-threshold current because the energy dissipation of a repeater-inserted spin interconnect is minimized around $\mathtt{r} = 0.2$. For the MMS mode, the electrical current is taken to be 3.3× the spin-threshold current for all interconnects except GNRs. For GNRs, the value of r for MMS mode is selected to be the same as that for the STS mode. The values are quoted for an interconnect length of 10 gate pitches at the 7.5 nm technology node. Both PF and EF for ASL circuit are much less than unity in the STS mode. The MMS mode improves PF and EF significantly for all spin interconnects. However, both EF and PF are still less than unity for all interconnects. Amongst the various materials studied for potential application as interconnects for the ASL circuit, it is GNRs that offers the best EF and PF in both STS and MMS modes of switching. Semiconducting interconnects have the highest energy dissipation owing to the requirement of a highly-resistive tunnel barrier at the interface, which increase the joule heating of the ASL circuit.

Table 29: Performance factor of ASL circuit with various interconnects. The interconnect length is selected to be 10 gate pitches at the 7.5 nm technology node. The CMOS diver size is taken to be $W/L = 1$. $I_{elec} = 5I_{spin,thres}$ for the STS mode. $I_{elec} = 3.3I_{spin,thres}$ for the MMS mode for all interconnects except GNRs. For GNRs, $I_{elec} = 5I_{spin,thres}$ in the MMS mode.

Material	**PF (STS)**	**PF (MMS)**
Copper ($R = 0.2$, $p = 0$)	8.11×10^{-6}	1.7×10^{-3}
Aluminum ($R = 0.2$, $p = 0$)	1.21×10^{-5}	2.6×10^{-3}
Silicon ($N_d = 10^{18}$ cm^{-3})	6.18×10^{-5}	5.2×10^{-3}
GaAs ($N_d = 10^{17}$ cm^{-3})	3.32×10^{-5}	6.7×10^{-3}
GaAs QW ($N_{IMP} = 10^{14}$ cm^{-3}, $N_s = 10^{10}$ cm^{-2})	2.13×10^{-5}	4.9×10^{-3}
GNR ($T_{TX} = 0.1$, $E_f = 0.2$ eV, $P_{GNR} = 0.2$)	1.11×10^{-5}	6.5×10^{-3}

Table 30: Energy factor of ASL circuit with various interconnects. The interconnect length is selected to be 10 gate pitches at the 7.5 nm technology node. The CMOS diver size is taken to be $W/L = 1$. $I_{elec} = 5I_{spin,thres}$ for the STS mode. $I_{elec} = 3.3I_{spin,thres}$ for the MMS mode.

Material	**EF (STS)**	**EF (MMS)**
Copper ($R = 0.2$, $p = 0$)	3.91×10^{-4}	0.1896
Aluminum ($R = 0.2$, $p = 0$)	5.82×10^{-4}	0.2807
Silicon ($N_d = 10^{18}$ cm^{-3})	2.98×10^{-6}	5.65×10^{-4}
GaAs ($N_d = 10^{17}$ cm^{-3})	1.60×10^{-6}	7.32×10^{-4}
GaAs QW ($N_{IMP} = 10^{14}$ cm^{-3}, $N_s = 10^{10}$ cm^{-2})	1.02×10^{-6}	5.29×10^{-4}
GNR ($T_{TX} = 0.1$, $E_f = 0.2$ eV, $P_{GNR} = 0.2$)	1.22×10^{-4}	0.071

6.4 System-Level Analysis of All-Spin Logic

In the preceding sections, it is shown that both the performance and the energy dissipation of spin and CMOS systems are highly dependent on the interconnect length. Any logic circuit has interconnects with drastically different interconnect lengths, where wire-length distribution is a function of the circuit architecture and complexity. To compare the system-level performance and energy dissipation of spin and CMOS systems, it is imperative that the stochastic models of wire-length distribution of random logic be taken into account. The stochastic wire-length distribution models were rigorously obtained by Davis et al. [43], [44]. The interconnect density function (IDF) is derived from the Rent's rule, which relates the number of input/output pins, T, to the number of gates, N, in a logic block, and it is mathematically given as

$$T = kN^{p_R}, \tag{186}$$

where k is the Rent's coefficient, and p_R is the Rent's exponent. The Rent's exponent captures the complexity of the circuit in that a less complex circuit has a lower value of p_R. The stochastic wire-length distribution model gives the number of interconnects of a given length in the logic block. The closed-form expression for the complete stochastic signal wiring distribution $i(l)$ is given as

$$\begin{aligned} &\text{Region I:} 1 \leq l \leq \sqrt{N} \\ i(l) &= \Gamma \frac{\alpha k}{2} \left(\frac{l^3}{3} - 2\sqrt{N} l^2 + 2Nl \right) l^{2p_R - 4}, \\ &\text{Region II:} \sqrt{N} \leq l \leq 2\sqrt{N}, \\ i(l) &= \Gamma \frac{\alpha k}{6} \left(2\sqrt{N} - l \right)^3 l^{2p_R - 4}, \end{aligned} \tag{187}$$

N is the number of gates in the random logic, Γ is a constant and is given in Eq. (188), p_R is the Rent's exponent, and $i(l)$ is the number of interconnects of length l per gate pitch. These expressions reveal the dependence of interconnect density on

interconnect length l in gate pitches.

$$\Gamma = \frac{2N(1 - N^{p_R - 1})}{-N^{p_R}\frac{1+2p_R-2^{2p_R-1}}{p_R(2p_R-1)(p_R-1)(2p_R-3)} - \frac{1}{6p_R} + \frac{2\sqrt{N}}{2p_R-1} - \frac{N}{p_R-1}}. \tag{188}$$

Figure 138 shows the IDF versus the interconnect length normalized to the gate pitch for two values of Rent's exponent. A lower value of Rent's exponent implies a less complex circuit and, therefore, has fewer interconnects of long length. Hence, the average interconnect length is smaller for a logic block with a lower value of the Rent's exponent.

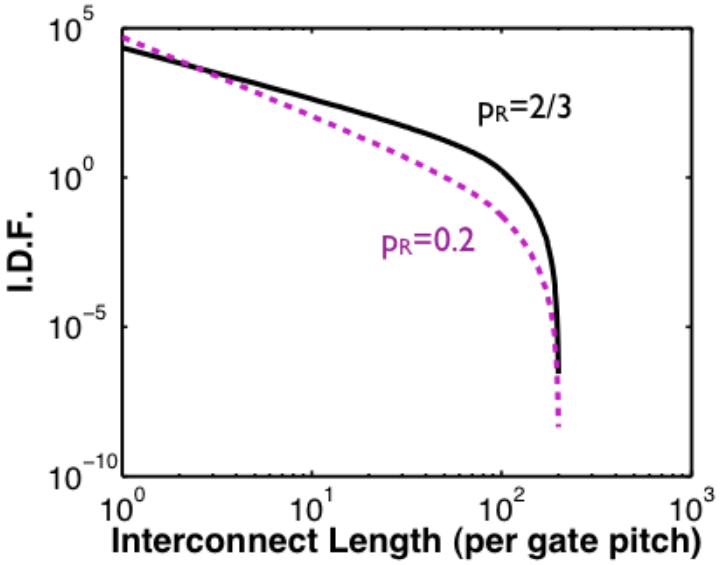

Figure 138: The interconnect density function for two values of Rent's exponent, p_R.

The average value of a quantity $f(l)$ that depends on the interconnect length in the random logic is evaluated as

$$\langle f(l) \rangle = \frac{\int_1^{2\sqrt{(N)}} f(l) \times i(l) dl}{\int_1^{2\sqrt{N}} i(l) dl}. \tag{189}$$

The average performance of CMOS system as a function of the logic block is plotted in Figure 139 for various values of Rent's exponent. The average delay of the CMOS system increases with an increase in the circuit size and the circuit complexity. The

rate of increase in the average delay of the CMOS system with circuit size is greater for a circuit with a higher value of the Rent's exponent. For a circuit size of 10,000 gates with $p_R = 0.55$, the average delay of the CMOS system with $W/L=1$ is 2.41 ps, while it is 0.93 ps for a 5× driver.

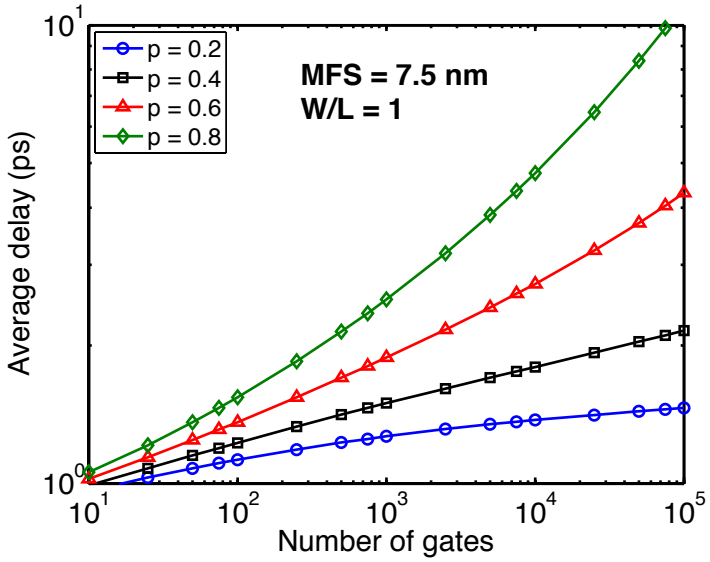

Figure 139: Average delay of CMOS system versus the circuit size for various values of Rent's exponent. The technology node is 7.5 nm.

The average energy dissipation of CMOS system versus the circuit size is shown in Figure 140 for various values of Rent's exponent, p_R. The average energy dissipation of the CMOS system increases gradually with an increase in circuit size for small values of p_R. However, the rate of increase in the average energy dissipation of the CMOS system with circuit size increases for higher values of Rent's exponent. For a circuit size of 10,000 gates with $p_R = 0.55$, the average energy dissipation of the CMOS system with $W/L=1$ is $5.92\times10^3 k_B T$, while it is $9.35\times10^3\ k_B T$ for a 5× driver.

The average performance and the average energy factors of the ASL system with various interconnects are tabulated in Tables 31 and 32, respectively. The circuit size is assumed to be composed of 1000 gates and the Rent's exponent is $p_R = 0.55$. The input electrical current for the STS mode is taken to be 5× the spin-threshold

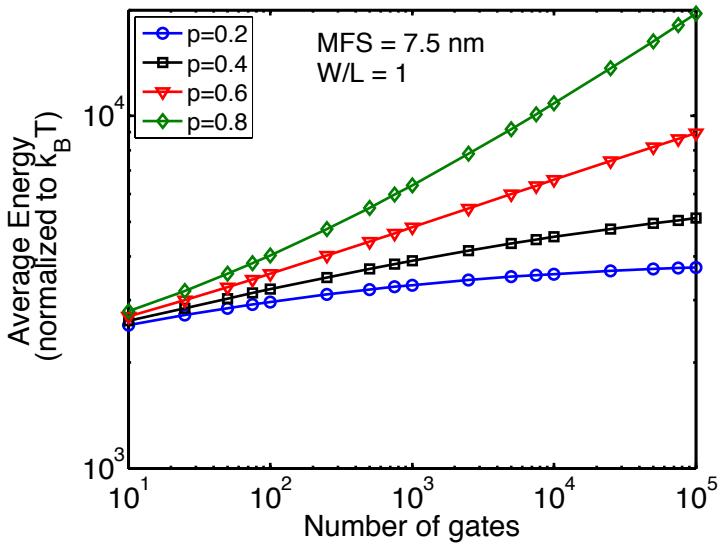

Figure 140: Average energy dissipation of CMOS system versus the circuit size for various values of Rent's exponent. The technology node is 7.5 nm.

current, while for the MMS mode the input electrical current is taken to be 3.3× the spin-threshold current for all interconnects except for GNRs. In the case of GNRs, the input electrical current for the MMS mode is taken to be the same as that in the STS mode. That is, $I_{elec} = 5 \times I_{spin,thres}$. For the CMOS circuit, the driver size is taken to be W/L = 1. The interconnect technology node is 7.5 nm.

In the next sub-section, the upper bound on the circuit size for an ASL system with GNR interconnects is quantified. The impact of circuit complexity and the material parameters of the interconnect on the maximum circuit size are also quantified.

6.4.1 Upper bound on circuit size of the ASL logic with GNR interconnects

As explained earlier in the chapter, repeaters are ubiquitous in spin logic. However, insertion of repeaters can limit the maximum circuit size of the ASL logic because only a certain fraction of the total number of gates in a circuit can be dedicated as repeaters, while most of the gates need to be utilized for implementing useful functionality.

Table 31: Average performance factor of the ASL system with various interconnects for both STS and MMS modes. $N = 1000$ gates and the Rent's exponent is $p_R = 0.55$.

Material	Average PF (STS)	Average PF (MMS)
Copper ($R = 0.2$, $p = 0$)	2.254×10^{-6}	2×10^{-3}
Aluminum ($R = 0.2$, $p = 0$)	4.783×10^{-6}	2.9×10^{-3}
Silicon ($N_d = 10^{18}$ cm^{-3})	4.247×10^{-5}	5.2×10^{-3}
Gallium Arsenide ($N_d = 10^{17}$ cm^{-3})	2.036×10^{-5}	7×10^{-3}
Gallium Arsenide QW	1.381×10^{-5}	5.4×10^{-3}
($N_{IMP} = 10^{14}$ cm^{-3}, $N_s = 10^{10}$ cm^{-2})		
Graphene Nanoribbons	1.742×10^{-5}	1.06×10^{-2}
($T_{TX} = 0.1$, $E_f = 0.2$ eV, $P_{GNR} = 0.2$)		

Table 32: Average energy factor of the ASL system with various interconnects for both STS and MMS modes. $N = 1000$ gates and the Rent's exponent is $p_R = 0.55$.

Material	Average EF (STS)	Average EF (MMS)
Copper ($R = 0.2$, $p = 0$)	1.106×10^{-4}	0.223
Aluminum ($R = 0.2$, $p = 0$)	2.35×10^{-4}	0.319
Silicon ($N_d = 10^{18}$ cm^{-3})	2.08×10^{-6}	5.79×10^{-4}
Gallium Arsenide	10^{-6}	7.688×10^{-4}
Gallium Arsenide QW	6.78×10^{-4}	6.019×10^{-4}
($N_{IMP} = 10^{14}$ cm^{-3}, $N_s = 10^{10}$ cm^{-2})		
Graphene Nanoribbons	1.92×10^{-4}	0.12
($T_{TX} = 0.1$, $E_f = 0.2$ eV, $P_{GNR} = 0.2$)		

The upper bound on the circuit size of the ASL circuit with GNR interconnects is shown in Figure 141 as a function of the Rent's exponent for various values of the spin-relaxation length in GNR assuming 10% of the gates are used as repeaters. It is found that for a given circuit complexity (i.e. fixed Rent's exponent), the maximum circuit

size is reduced for a lower spin-relaxation length. Increase in circuit complexity also lowers the upper bound on the circuit size. As the value of Rent's exponent increases from 0.2 to 0.8, N_{max} reduces from 75 gates to 45 gates for L_{SN} = 18 μm for the parameters selected for this simulation. For the same change in p_R, N_{max} reduces from 70 gates to 40 gates for L_{SN} = 5 μm.

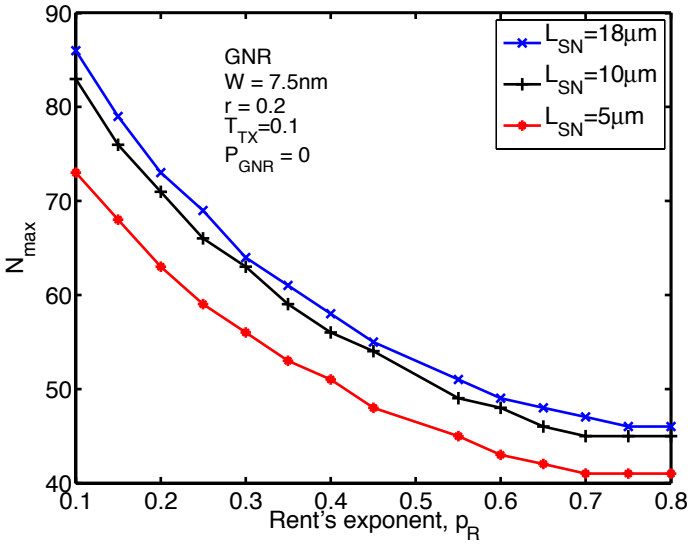

Figure 141: Maximum circuit size versus Rent's exponent for an ASL circuit with GNR interconnects. Various spin-relaxation lengths in the interconnect are considered. 10% of the total gates are considered to be dedicated as repeaters.

The impact of receiver sensitivity on the upper bound of circuit size is shown in Figure 142. It is assumed that only 10% of the total number of gates are dedicated as repeaters. A decrease in the receiver sensitivity or an increase in the ratio $r = I_{spin,thres}/I_{elec}$ drastically lowers the maximum circuit size. However, the upper bound on circuit size improves when the transmission coefficient is lowered at the transmitter. This is because a lower T_{TX} improves spin filtering of electrons, which helps to improve the critical interconnect length and reduce the number of repeaters that need to be inserted along the interconnect. For T_{TX} = 0.01, the upper bound on circuit size reduces from 10^5 gates to 2500 gates as r increases from 0.1 to 0.3.

However, for $T_{TX} = 0.1$, the upper bound on circuit size is below 100 gates even for a low value of $r = 0.1$.

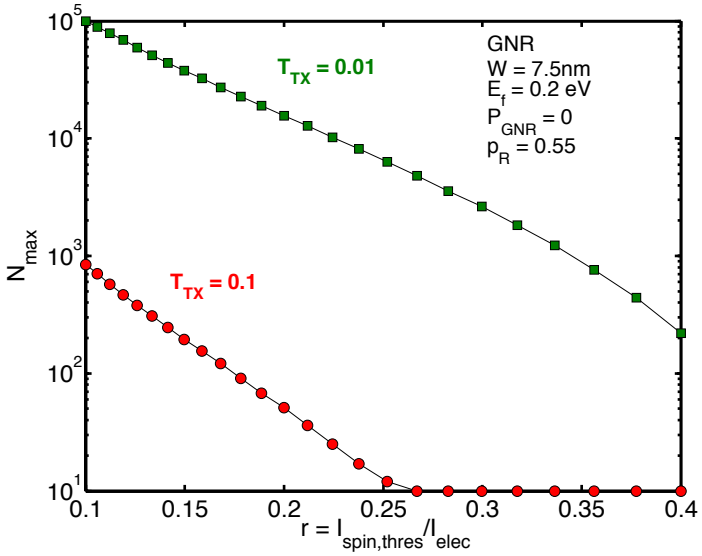

Figure 142: Upper bound on the circuit size of the ASL system with GNR interconnects as a function of the inverse of the receiver sensitivity for various values of L_{SN}. 10% of the total gates are considered to be dedicated as repeaters.

The impact of dimensional scaling on the upper bound of circuit size of the ASL circuit with GNR interconnects is shown in Figure 143 for various values of P_{GNR} and T_{TX}. It is assumed that only 10% of the total gates are dedicated as repeaters. In the absence of any edge scatterings ($P_{GNR} = 0$), the upper bound on circuit size is independent of the interconnect width. However, for a non-zero value of P_{GNR}, the upper bound on circuit sizes reduces as the interconnect width scales down. For example, N_{max} reduces from 7000 gates to 800 gates as the width scales from 25 nm to 5 nm for $T_{TX} = 0.01$. A lower value of N_{max} means that the spin signal needs to be frequently converted into an electrical signal. However, frequent signal conversion also entails energy dissipation and circuit-area overhead.

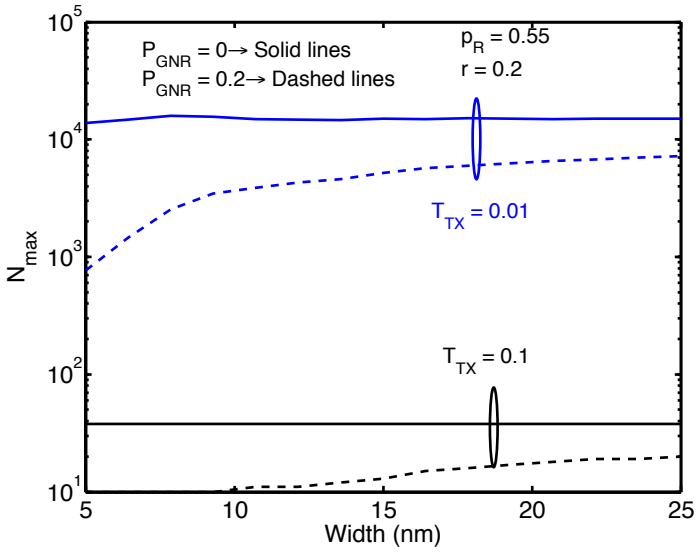

Figure 143: Upper bound on circuit size of the ASL circuit versus the GNR interconnect width for various values of P_{GNR} and T_{TX}. 10% of the total gates are considered to be dedicated as repeaters.

6.5 Conclusions

In this chapter, the circuit- and system-level analyses of the all-spin logic (ASL) are presented. Due to spontaneous spin flipping occurring within the interconnect, spin signal decays appreciably as it reaches the receiver electrode. If the spin current reaching the receiver threshold is not sufficient to toggle the receiver, then spin repeaters must be inserted along the interconnect at a critical length to boost the spin signal. One of the crucial findings of this chapter is that the relationship between the critical interconnect length and material and design parameters of the ASL circuit is established. It is found that a degradation in the receiver sensitivity degrades the critical interconnect length for all interconnect materials. It is shown that the GNRs offer the best-case critical interconnect length amongst the various metallic and semiconducting interconnects analyzed in this chapter.

In spin interconnects, repeaters may also be inserted to minimize the delay of the circuit. In this case, the optimal repeater insertion frequency has been determined

for various interconnect materials considering both full spin-torque assisted (STS) and mixed-mode switching (MMS) schemes for the nanomagnet. It is found that the interconnect length does not significantly change the ratio of optimal to critical repeater-insertion frequency. An optimal value of the input electrical current to minimize the energy dissipation of the ASL circuit with both STS and MMS switching modes is determined for various interconnect materials. It is found that the optimal value of the electrical current is largely independent of the interconnect length. This important finding can help circuit designers to choose a constant value of input electrical current to yield minimum energy dissipation without having to tweak the input electrical current with interconnect length. The energy-delay landscape of the ASL circuit is found to exhibit a minimum energy point. This is in contrast to the energy-delay landscape obtained for CMOS circuits.

A system-level analysis shows that the average performance and the average energy dissipation of the ASL circuit is far inferior to those of its CMOS counterparts, especially when the STS mode of switching is considered. The MMS mode shows a drastic improvement in these figures of merit for the ASL circuit. Nonetheless, even in the MMS mode, the average performance and average energy dissipation of the ASL circuit are inferior compared to those of the CMOS circuit. Amongst the various interconnect materials analyzed, it is demonstrated that an ASL circuit with graphene-based interconnects has the lowest circuit and system-level energy dissipation. Since the dominant component of the delay and energy dissipation in a spin circuit comes from the nanomagnet, it is imperative that parallelism of computation be in-built into the architecture of the spin circuit.

Another major limitation of spin-based circuits comes from the requirement of spin repeaters. The fact that spin signal degrades as it is transported through long channels necessitates the insertion of spin repeaters to boost the spin signal. In a real circuit composed of many gates, it must be ensured that only a certain fraction

of gates are dedicated as repeaters, while most gates are used towards implementing useful functionality. Our simulations show that with a high spin filtering of electrons at the nanomagnet-graphene interface and for less complex circuits having a lower value of Rent's exponent, the upper bound on the circuit size can be improved to more than 1000 gates.

It must be noted that, in principle, designing a fully-optimized ASL circuit requires a multi-variable optimization with respect to the nanomagnet material & dimensions, interconnect material & dimensions, doping concentration for semiconducting interconnects, and the interface resistance-area product. Even though this is beyond the scope of the present thesis, our research has demonstrated the major limitations of the all-spin logic at both the circuit and system levels.

CHAPTER VII

CONCLUSION AND OUTLOOK

This chapter concludes the dissertation by first reviewing the salient contributions of the research work. Important insights and recommendations are also provided. This is followed with a description of possible extensions of the work conducted here into future endeavors.

7.1 Conclusion

The objective of this dissertation is to evaluate the opportunities, advantages, and limits of interconnects in post-CMOS logic that can augment or eventually replace the CMOS logic. Post-CMOS devices are envisaged on the idea of using state variables other than electron charge to store and manipulate information. To this date, various potential candidates have emerged as *the state variable of the future*. Some noteworthy examples include the electron charge, pseudospin in graphene, excitons, phonons, domain walls, and photons. Amongst these state variables, electron spin is the most studied with potential advantages in terms of its robustness and non-volatility. Since electrons inherently possess both charge and spin, it is possible to conceive a logic system where spin is used to enhance the functionality provided only by the electron charge. The interconnections form an integral component of any logic system as they provide the physical medium to carry information between the devices in the system. Most research in post-CMOS logic is focused only on demonstrating theoretically or experimentally novel logic devices with alternate state variables, while almost negligible research has been conducted on transport of novel state variables. To this end, this research focusses primarily on developing physical models for transport of novel state variables to evaluate the interconnect limits in future technology options.

This is, in part, also motivated by the fact that electrical interconnects in the current CMOS logic are a major bottleneck in gigascale integration. Interconnects add delay in critical paths and also consume more than 50% of the total power dissipated in a microprocessor. Hence, a thorough analysis of novel interconnects is imperative at this time. To accomplish the research goal, five contributions have been identified:

1. Identifying transport mechanism for carrier transport in novel interconnects-modeling delay and energy dissipation as a function of interconnect length; concept of area scaling

2. Modeling transport parameters in metallic, semiconducting, and GNR interconnects

3. Modeling spin-relaxation length in metallic, semiconducting, and GNR interconnects

4. Spin injection and transport efficiency in all-spin logic based on standard model of spin injection

5. Circuit- and system-level analyses of all-spin logic: optimal spin-repeater insertion frequency; upper bound on circuit size of ASL

In conclusion, 1) a mapping between the state variable and the possible transport mechanism that can help to communicate information encoded in the state variable is established. There are two major transport mechanisms that can be used in novel interconnects: (i) particle-based (diffusion, drift, and ballistic) and (ii) wave-based (spin waves and electromagnetic waves). The physical equations governing the particle/wave transport are presented. Simple mathematical expressions for evaluating the delay and the energy dissipation of the novel interconnects are provided. The compact physics-based models enable projection of interconnect performance for future technology options. A vital contribution of Chapter I is provided by *the concept of*

area scaling. While it is demonstrated that interconnects in novel logic will continue to be a major bottleneck with respect to performance and energy dissipation of the novel logic, scaling the footprint of novel devices or using fewer gates to implement a given function can help to shorten interconnect lengths between devices. This concept termed as "area scaling" can be extremely useful to improve the performance of the novel circuit while reducing the energy dissipated in interconnects.

2) Even though spin-based devices and circuits have been consistently gaining popularity, there are no readily available compact models of spin-transport parameters in materials that can serve as the channel or the interconnect for these spin-based devices. Most theoretical studies assume constant values for spin-transport parameters, whereas, in reality, these parameters vary significantly with channel dimensions, size effects, temperature, and also with the dopant concentration for semiconducting channels. Compact physics-based models of spin diffusivity, mobility, and material resistivity have been obtained for metallic interconnects (copper and aluminum), semiconducting interconnects (silicon and gallium arsenide), and graphene nanoribbons as a function of dimensional scaling in the presence of size effects. The models have been calibrated exhaustively with the existing experimental data. The generic nature of the models allows us to study/analyze spin-based devices, such as the all-spin logic device.

3) Electrons tend to lose their spin orientation over time, which is characterized by a time constant called the spin-relaxation time. The distance through which electrons diffuse before losing spin orientation is called the spin-relaxation length. In reality, both spin-relaxation time and length are highly dependent upon the cross-sectional dimensions of the spin device and the presence of size effects. The key contribution of this task is to provide compact physics-based models of spin relaxation time and length in various materials such that the models can accurately capture the impact of dimensional scaling of spin devices. The simple, compact nature of these models

enables us to embed them in developing CAD tools to analyze spin circuits. *Amongst the various materials studied, it is graphene nanoribbons that have the longest spin-relaxation length, which is nearly independent of size effects. However, the spin-relaxation length in graphene depends quite strongly on the nature of the spin-orbit coupling of adatoms in the material. The spin-relaxation length of electrons in silicon reduces with an increase in doping concentration. However, in the case of bulk gallium arsenide that is non-degenerately doped, spin-relaxation length becomes independent of doping concentration and saturates to 0.5* μm *and varies as* $1/T$*, where* T *is the lattice temperature. Metals like Cu and Al have an exceptionally short spin-relaxation length for interconnect applications. In addition, the dimensional scaling further degrades the spin-relaxation length and limits it to approximately 100 nm for a 7.5 nm wide channel.*

4) The physical models developed in Tasks 2 and 3 are applied to evaluate the efficiency of spin injection and transport (SITE) in a non-local spin-torque based device, also called the all-spin logic device. The SITE captures the losses in the spin signal encountered upon injection from a nanomagnet into the interconnect and also the loss while transporting the signal through the interconnect. *It is shown conclusively that use of a tunnel barrier for the ASL geometry with either metallic or semiconducting interconnects is important to increase the value of SITE.* For device applications, channels are relatively short and as such the SITE is only governed by the injection efficiency. However, for interconnect applications, there is a significant contribution to SITE that arises from losses generated while transporting the spin signal through an interconnect whose length is longer than the spin-relaxation length. *For silicon interconnects, an optimal doping density is identified that maximizes the SITE of the ASL device. The optimal doping density is found to depend upon the length of the interconnect. However, the optimal doping density is less than* 3×10^{18} cm^{-3} *for lengths longer than 1* μm*. In the case of GaAs interconnects, an increase*

in doping density leads to an increase in the value of SITE of the ASL device, and no optimal doping density exists. In the case of graphene without any adatoms, the spin-relaxation length is found to be independent of width and edge roughness and is $\approx$ 18 μm as obtained in Task 3. *Hence, in the case of ASL device with GNR interconnects, SITE is largely governed only by the injection efficiency. It is found that SITE improves with a reduction in the transmission coefficient at the interface, which helps to improve the spin filtering of electrons.*

5) An ASL circuit incorporating the nanomagnet dynamics is analyzed for full-spin torque and mixed-mode switching schemes of the nanomagnet. The critical interconnect length for repeater insertion is determined as a function of dimensional scaling of the interconnect, size effects, and receiver sensitivity. The critical interconnect length rapidly degrades with a drop in receiver sensitivity and becomes too short to be useful for interconnect applications. As the delay of spin interconnects increases quadratically with interconnect length, spin repeaters may also be inserted to minimize the delay of the spin interconnect. *The optimal repeater insertion frequency with respect to the critical repeater insertion frequency is found to be relatively insensitive to the interconnect length, and it is also insensitive to the receiver sensitivity when the input electrical current is chosen such that it is less than 5× the spin-threshold current of the receiver.* Using physical models of nanomagnet and the interconnect switching, the performance and the energy dissipation of the ASL circuit and the CMOS circuit are compared at the 7.5 nm technology node. The ASL circuit with GNR interconnects has the best-case performance and energy dissipation when the mixed-mode switching of the nanomagnet is considered. The energy-delay landscape of the ASL circuit is compared with that of the CMOS circuit. *It is found that the spin circuit, unlike the CMOS circuit, exhibits a minimum energy point in its energy-delay landscape.* At the system level, stochastic wire-length distribution models are used to evaluate the average performance and energy dissipation of the ASL system

as a function of the circuit size and complexity. An upper bound on the circuit size of the ASL system is found as a function of material and design parameters in the system by assuming that only a certain fraction of the total number of gates in the system are dedicated as repeaters. *It is shown that the maximum circuit size of the ASL system is limited by the repeater-insertion requirements. For an ASL system with GNR interconnects in which only 10% of the gates are dedicated as repeaters, the upper bound on the circuit size can be as small as 100 gates. Unless circuits with lower complexity or shorter interconnects are designed, it would be challenging to increase the maximum circuit size of the ASL system. In this sense, parallelism of operation may be the key to harnessing the potential of the spin logic.*

The research conducted here is instrumental in pointing out the advantages, limits, and challenges of the post-CMOS logic, in particular the spin-based logic.

7.2 Future Work

7.2.1 Incorporating electric-field effects in spin devices with semiconducting channels/interconnects

In semiconductors, the spin polarization is usually assumed to obey the same diffusion equation as in metals. This equation is given as

$$\nabla^2 (\mu_\uparrow - \mu_\downarrow) - \frac{(\mu_\uparrow - \mu_\downarrow)}{L_s^2} = 0. \tag{190}$$

This equation was discussed in Chapter V. However, this equation is valid only when the electric field in the system is effectively screened. As such, this equation works only in the case of metals. In the case of semiconductors, a more general form of the equation is given as

$$\nabla^2 (n_\uparrow - n_\downarrow) + \frac{eE}{k_B T}.\nabla (n_\uparrow - n_\downarrow) - \frac{n_\uparrow - n_\downarrow}{L_s^2} = 0, \tag{191}$$

where $(n_\uparrow - n_\downarrow)$ is the difference in the concentration of up-spin and down-spin electrons, L_s is the intrinsic spin-relaxation length of electrons (discussed in Chapter IV),

and E is the electric field acting on the spin carriers. The central role of the electric field in semiconductors is that the spin motion will now be characterized using two distinct spin-relaxation lengths: (i) up-stream spin-relaxation length, L_u and (ii) down-stream spin-relaxation length, L_d. In principle, L_u can be much shorter than L_s in the high-field regime. This fact can lead to significant difference in the injection and transport efficiency of electron spins through a semiconducting interconnect on which an external electric field has been applied, such as the drift geometry (see Figure 18 in Chapter II). The critical electric field, E_c is given as

$$E_c = \frac{1}{eL_s}\left(\frac{\mu}{eD}\right)^{-1}, \tag{192}$$

where μ and D are the charge mobility and diffusivity, respectively. The critical electric field as a function of doping concentration in Si and GaAs is plotted in Figure 144. For electric fields greater then E_c, the drift term in Eq. (191) is more important than the diffusive term and hence, neglecting electric-field effects in this regime is not justified. The critical electric fields obtained for silicon and gallium arsenide in Figure 144 are realistic electric fields under which the current spintronic devices are expected to operate [243].

The up-stream and down-stream spin-relaxation lengths differ significantly from L_s in the high-field regime, and the mathematical expressions for these length scales are given as

$$L_d = \left(\frac{-|eE|}{2}\frac{\mu}{eD} + \sqrt{\left(\frac{|eE|}{2}\frac{\mu}{eD}\right)^2 + \frac{1}{L_s^2}}\right)^{-1}, \tag{193a}$$

$$L_u = \left(\frac{|eE|}{2}\frac{\mu}{eD} + \sqrt{\left(\frac{|eE|}{2}\frac{\mu}{eD}\right)^2 + \frac{1}{L_s^2}}\right)^{-1}. \tag{193b}$$

In Figure 145, the ratios L_u/L_s and L_u/L_d are plotted as a function of doping concentration in both silicon and gallium arsenide for an electric field of 1000 V/cm. This figure shows that there could be a significant variation in L_u and L_d relative to the intrinsic L_s when an electric field is applied on the semiconducting interconnect.

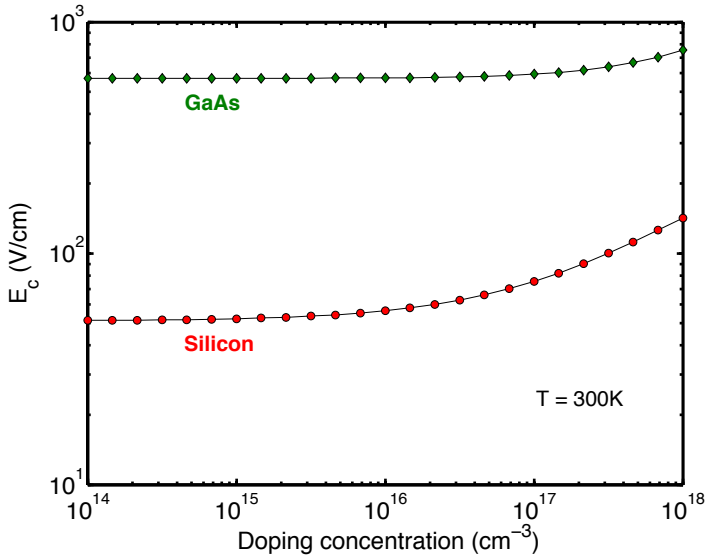

Figure 144: Critical electric field versus doping concentration in semiconducting interconnects.

Hence, electric-field effects must be accounted for in semiconductors to study the spin transport through semiconductors.

In semiconductors, the relationship between the splitting of the spin quasi-chemical potentials of the up-spin and down-spin electrons is not linearly related to the concentration of the up-spin and down-spin carriers. A general relationship between $n_\uparrow/n_\downarrow$ and $\mu_\uparrow/\mu_\downarrow$ is given as

$$n_\uparrow = n_\uparrow^\circ \left(\exp\left(\frac{\mu_\uparrow - \mu_0}{k_B T} \right) - 1 \right), \tag{194a}$$

$$n_\downarrow = n_\downarrow^\circ \left(\exp\left(\frac{\mu_\downarrow - \mu_0}{k_B T} \right) - 1 \right), \tag{194b}$$

where $n_\uparrow^\circ$ and $n_\downarrow^\circ$ are the equilibrium concentrations of up-spin and down-spin carriers, respectively. As the relationship between the spin carrier concentration and the spin quasi-chemical potential is non-linear, Eq. (191) cannot be simply converted into a linear differential equation for the spin quasi-chemical potential; this is unlike the case for metals where a linear relationship exists between the spin carrier concentrations and the spin quasi-chemical potentials.

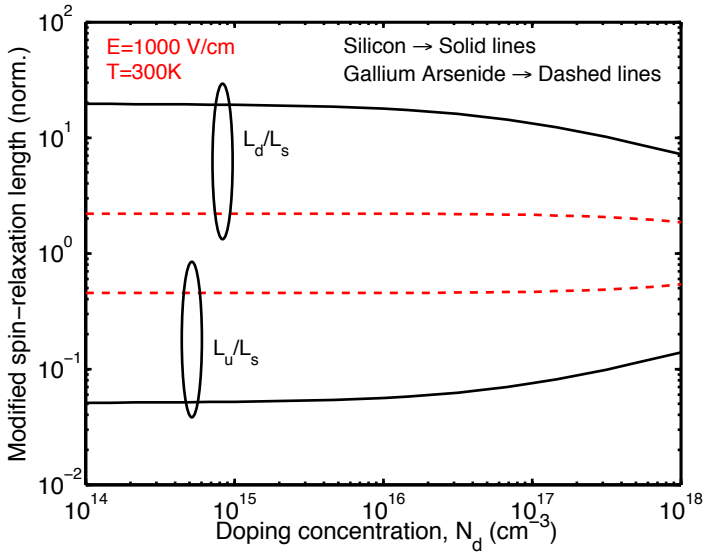

Figure 145: Up-stream and down-stream spin-relaxation lengths versus doping concentration for silicon and gallium arsenide with an electric field of 1000 V/cm.

A Schottky barrier is also formed at the interface between the magnet and the semiconductor in both diffusion and drift-based geometries of the spin logic. Transport through the Schottky barrier is comprised of (i) thermionic emission, (ii) diffusion, and (iii) tunneling currents. Hence, the conductance at the interface for up-spin and down-spin carriers cannot be assumed independent of voltage and temperature. The effects of band bending in the semiconductor channel along with an accurate analysis of Schottky barrier will be instrumental in accurately capturing the spin transport through spin-based devices using semiconducting channels and interconnects.

7.2.2 Signal conversion

For relatively long interconnects, it might be more energy efficient to convert the spin signal to an electrical signal. To identify the length beyond which signal conversion is advantageous, the energy overhead for signal conversion needs to be modeled. The circuit that can be used to estimate the conversion energy is shown in Figure 146.

The information stored in the output magnet comes from the spin current from the previous stage. The reference layer is pinned in a particular orientation. The combination of the reference layer, the tunnel barrier, and the output layer form a tunnel magnetoresistance (TMR) device and its output can be converted to a digital signal using a sense amplifier. The active and standby power in the senses amplifier and the TMR need to be modeled and the circuit can be designed for minimum energy per bit operation.

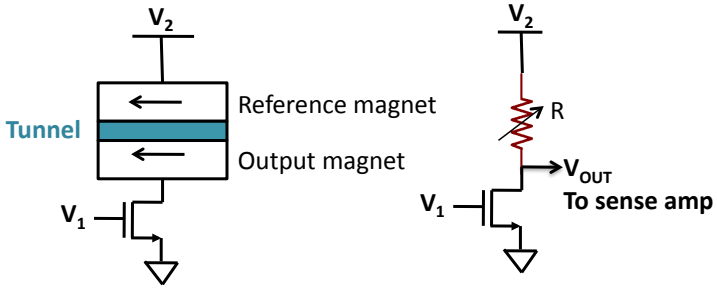

Figure 146: The LHS figure shows a tunnel magnetoresistance (TMR) device and an NFET connected to it that can be used to read information available in the magnetization of the output magnet. The circuit representation is shown in RHS figure. The voltage V_{OUT} is fed into a sense amplifier, which can digitize the information in V_{OUT} signal.

A first-level analysis of the energy consumed in converting the resistance of the TMR device into the voltage signal V_3 is given below. The energy dissipation is given as

$$E = \int_0^{t_f} i_2 V_2 dt, \tag{195}$$

where E is the energy drawn from the supply source V_2, i_2 is the current drawn from V_2, and t_f is the time duration for which the current is supplied by the source voltage. The current i_2 is given as

$$i_2 = i_1 + i_3 = \frac{V_2 - V(t)}{R}, \tag{196}$$

where i_1 is the current through the NFET in Figure 146, i_3 is the current through the capacitor at the output node, and $V(t)$ is the time-dependent voltage at the output

node. If the NFET is assumed to be in the linear mode of operation, then the current through the NFET is given as

$$i_1 = k'V(t), \tag{197}$$

where k' depends upon the technology parameters (mobility and oxide capacitance) and design parameter W/L (width-to-length ratio of the NFET). The current i_3 through the output capacitance, C_{out}, is given as

$$i_3 = \frac{dQ}{dt} = C_{out}\frac{dV(t)}{dt}. \tag{198}$$

Using Eqs. (195)-(198), the energy dissipation is given as

$$E = V_2^2\frac{k'}{1+k'R}t_f + \frac{C_{out}V_2}{1+k'R}V_3, \tag{199}$$

where V_3 is given as

$$V_3 = \frac{\zeta V_2}{1+k'R} \tag{200}$$

The pre-factor ζ dictates that the voltage is shut off after a time duration of t_f such that the final voltage never exactly reaches exactly 100% of the steady state value, which would have taken infinite time because of the RC charging time constant at the output node. Invoking the pre-factor ζ, the time t_f is given as

$$t_f = \frac{C_{out}V_2^2}{1+k'R}\left(k'R\ln\left(\frac{1}{1-\zeta}\right)+\zeta\right). \tag{201}$$

7.2.3 Self consistent simulation of nanomagnets and interconnects

The phenomenological equation governing the nanomagnet dynamics is the modified Landau-Lifschitz-Gilbert equation with the inclusion of the spin-torque term. In a real circuit with several magnets and interconnects, the spin transport through the interconnect and the dynamics of the nanomagnet are coupled together. This is because the current passing through the circuit depends upon the direction of the

nanomagnet magnetization, while the direction of the nanomagnet magnetization is itself modified by the spin current injected into it. Therefore, this self consistency of the problem must be addressed to accurately obtain the time dependent profiles of the spin current in every region of the spin circuit.

7.2.4 SPICE macro models of spin circuits

Analyzing the time-dependent evolution of spin concentration and spin current in a metallic or a semiconducting channel is the key towards designing a fully-optimized hybrid spin/CMOS circuit. However, designing complete circuits composed of several spintronic and electronic blocks on the same platform using mathematical tools like MATLAB is a daunting challenge. Towards this end, it would be extremely useful to represent spin circuits using SPICE macro models. These macro models can later be used as a building block in a hierarchical simulation tool for analyzing spintronic circuits and systems. The models will also provide a fast and easy way to design and optimize various technology parameters for spintronic interconnects. The models will also offer a better insight into spintronic interconnects as they represent spintronic interconnects with electrical components that are more familiar for most circuit designers.

Recently, SPICE macro models for the nanomagnet have been developed in [138]. The attractive feature of these models is that they can be easily combined with the spin interconnect SPICE macro models to run a complete self consistent simulation of nanomagnet and interconnect dynamics as outlined in the previous section. Using the SPICE macromodels, some basic, representative circuit blocks (adders and multipliers) in spin logic can be simulated. Such simulations can provide important insights regarding the size and complexity of spintronic logic blocks and the interconnect length beyond which conversion from spin domain to electrical domain is beneficial. This task can utilize the results obtained in Sections 7.2.2 and 7.2.3.

7.2.5 Novel architectures

With the exception of graphene-based spin logic, it has been shown that spin logic is much slower and consumes much more energy when compared to its CMOS counterpart. Hence, a promising architecture for spintronic systems must meet the following requirements: (i) implement massive concurrency to mask the low computation and communication speeds, (ii) Implement highly localized computation to avoid long interconnects which require repeaters or spin-to-electrical signal convertors, and (iii) take advantage of the non-volatile nature of spin-based devices. An example of such an architecture is the array processor in which the arrays operate either in parallel or in pipeline. Each processor is connected only to its nearest neighbor [118]. Array processors with spin logic can be utilized towards specific applications such as matrix manipulation, video filtering, data processing etc. [118]. A recent proposal on using electron spin computation to implement non-Boolean, analog mode, majority evaluation is the neuromorphic architecture using lateral spin valves [194]. This architecture can be used for analog data sensing, data conversion, cognitive computing, associative memory, and analog and digital signal processing.

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VITA

Shaloo Rakheja was born in Kanpur, India in August 1982. In May of 2005, she received a Bachelor of Technology in Electrical Engineering from the Indian Institute of Technology, Kanpur. She worked as a Component Engineer at Intel, Bangalore in 2005 and later as an Analog Engineer at Freescale Semiconductor, Noida from 2006 to 2007. In August of 2007, she had the privilege to join Professor Azad Naeemi's research group. She received a Master of Science in Electrical and Computer Engineering from the Georgia Institute of Technology in May 2009. Over the last five years, she has co-authored seventeen international conference and refereed journal publications. She has also co-authored two book chapters and contributed to the chapter on Emerging Interconnect in ITRS 2011. She received the Intel PhD Fellowship for the academic year 2011-2012. She also received the ECE Graduate Research Assistant Excellence Award for the academic year 2011-2012. Her research efforts have focused on evaluating the interconnection aspects of post-CMOS nanoelectronic devices with a special emphasis on spintronics. Her current research interests include modeling the electron spin transport phenomena through metallic, semiconducting, and carbon-based materials.